LP3923 Cellular Phone Power Management Unit

Check for Samples: LP3923

FEATURES

- **Integrated Li-Ion Battery Charger with Power FET, Thermal Regulation and 28V OVP**
- **Six Low-Noise LDOs, Two LILO LDOs**
  - **3 x 300 mA**
  - **4 x 150 mA**
  - **1 x 80 mA**
- **One High Efficiency Synchronous Magnetic Buck Regulators, I_{OUT} 700 mA**
  - **High Efficiency PFM Mode @low I_{OUT}**
  - **Auto Mode PFM/PWM Switch**
  - **Low Inductance 2.2 µH @ 2 MHz Clock**
- **I^2C-compatible Interface for Controlling LDO Outputs and Charger Operation**
- **Thermal Shutdown with Early Warning Alarm**
- **Under-Voltage Lockout**
- **30-bump 3.0 x 2.5 mm DSBGA Package**

APPLICATIONS

- **Cellular Handsets**

KEY SPECIFICATIONS

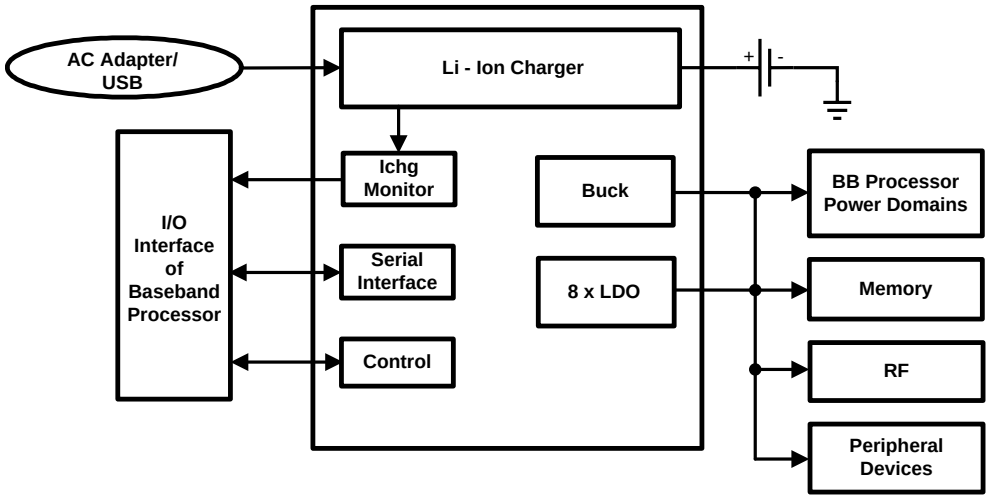
- **50 mA to 1200 mA Charging Current**
- **3.0V to 5.5V Input Voltage Range**
- **135 mV typ. Dropout Voltage @ 300 mA LDOs**
- **2% (typ.) Output Voltage accuracy on LDOs**
- **700 mA (typ.) Buck Regulator**

DESCRIPTION

The LP3923 is a fully Integrated Power Management Unit (PMU) designed for CDMA cellular phones.

The LP3923 PMU contains a fully integrated Li-Ion battery charger with power FET and over-voltage-protection (OVP), one Buck regulator, 8 low-noise low-dropout (LDO) voltage regulators, and a high-speed serial interface to program on/off conditions and output voltages of individual regulators, and to read status information of the PMU. Two LILO (low-input, low-output) type LDOs with separate power input provide an application option for pre-regulated high efficient power management for longer battery life.

System Diagram



DESCRIPTION (CONTINUED)

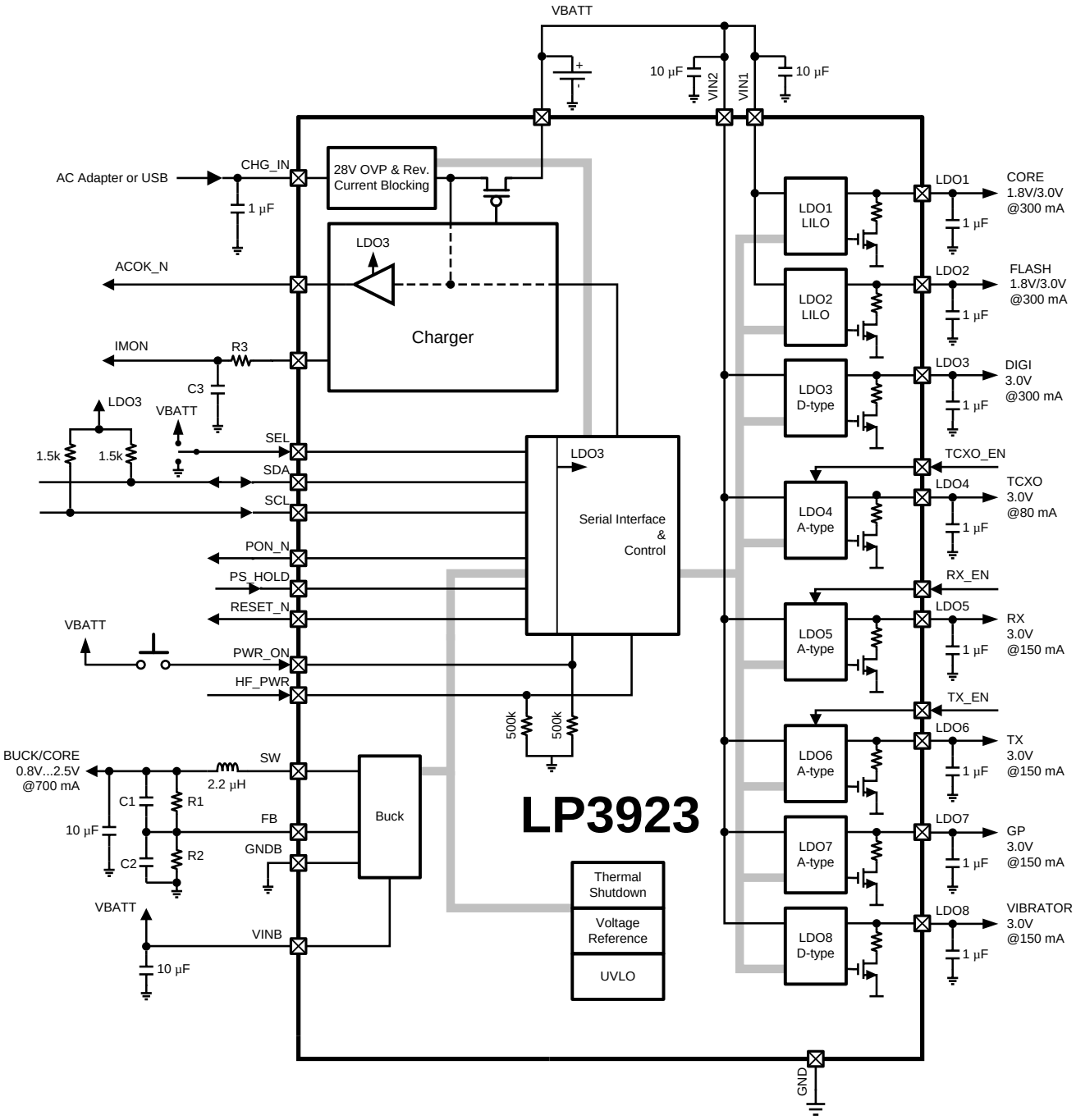
The Li-Ion charger can safely charge and maintain a single cell Li-Ion battery operating from an AC adapter. The charger integrates a power FET, a reverse current blocking diode, a sense resistor with current monitor output, and requires only a few external components. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature.

A built-in Over-Voltage Protection (OVP) circuit at the charger inputs protects the PMU from input voltages up to +28V, eliminating the need for any external protection circuitry.

Buck regulator has an automatic switch to PFM mode at low load conditions providing very good efficiency at low output currents. An external divider circuitry provides user defined buck output voltage.

A-type LDO regulators provide excellent PSRR and very low noise, 10 µV typ., ideally suited for supplying voltage to RF and other analog sections.

Typical Application Diagram



Device Pin Diagram

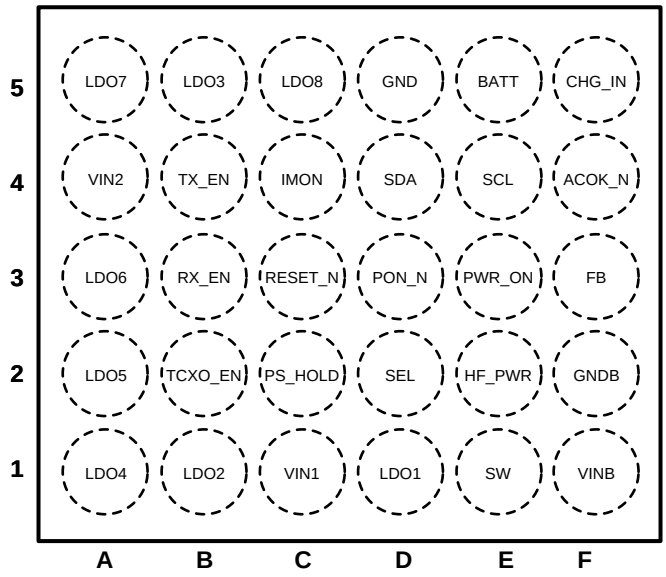


Table 1. LP3923 PIN DESCRIPTIONS(1)

Pin Number	Name	Type	Description
A1	LDO4	A	LDO4 Output
A2	LDO5	A	LDO5 Output
A3	LDO6	A	LDO6 Output
A4	VIN2	P	Input for LDO3 -LDO8
A5	LDO7	A	LDO7 Output
B1	LDO2	A	LDO2 Output
B2	TCXO_EN	DI	Enable control input for LDO4. HIGH = Enable, LOW = Disable (SLEEP Mode).
B3	RX_EN	DI	Enable control input for LDO5. HIGH = Enable, LOW = Disable.
B4	TX_EN	DI	Enable control input for LDO6. HIGH = Enable, LOW = Disable.
B5	LDO3	A	LDO3 Output
C1	VIN1	P	Input for LDO1 and LDO2
C2	PS_HOLD	DI	Power Supply Hold Input
C3	RESET_N	DO	Reset Output. Pin stays LOW during power up sequence
C4	IMON	A	Charging current monitor output. This pin presents an analog voltage representation of the charging current.
C5	LDO8	A	LDO8 Output
D1	LDO1	A	LDO1 Output
D2	SEL	DI	LDO1 and LDO2 default voltage selection.
D3	PON_N	DO	State of PWR_ON inverted. Digital output referred to LDO3.
D4	SDA	DI/O	Serial Interface, Data Input/Output Open Drain output, external pull up resistor is needed, typ. 1.5 kΩ.
D5	GND	G	IC Ground pin
E1	SW	A	Buck Output

(1) A: Analog Pin D: Digital Pin I: Input Pin DI/O: Digital Input/Output Pin G: Ground O: Output Pin P: Power Connection

Table 1. LP3923 PIN DESCRIPTIONS(1) (continued)

E2	HF_PWR	DI	Power up sequence starts when this pin is set HIGH. Internal 500 kΩ pull-down resistor.
E3	PWR_ON	DI	Power up sequence starts when this pin is set HIGH. Internal 500 kΩ pull-down resistor.
E4	SCL	DI	Serial Interface Clock input.
			External pull up resistor is needed, typ. 1.5 kΩ.
E5	BATT	P	Main battery connection. Used both as a power connection for current delivery to the battery and as a voltage sense connection to monitor the battery charge level.
F1	VINB	P	Input for Buck
F2	GNDB	G	Power Ground for Buck
F3	FB	A	Buck Feedback pin
F4	ACOK_N	DO	AC Adapter indicator, LOW when V_{CHG_IN} is above its trip point
F5	CHG_IN	P	DC power input to charger block from AC adapter or USB

Device Description

The LP3923 Charge Management and Regulator Unit is designed to supply charger and voltage output capabilities for mobile systems, e.g. CDMA handsets. The device provides a Li-Ion charging function and 8 or 9 regulated outputs. Communication with the device is via an I^2C compatible serial interface that allows function control and status read-back.

The battery charge management section provides a programmable CC/CV linear charge capability and end of charging current threshold. Following a normal charge cycle a maintenance mode utilizing programmable restart voltage levels enables the battery voltage to be maintained at the correct level. Power dissipation is thermally regulated to obtain optimum charge levels over the ambient temperature range.

CHARGER FEATURES

- Pre-charge, CC, CV and Maintenance modes
- Integrated FET
- Integrated Reverse Current Blocking Diode
- Integrated Sense Resistor
- Thermal Regulation
- Charging Current Monitor Output
- Programmable charging current 50 mA - 1200 mA with 50 mA steps
- Default CC mode current 400 mA
- Pre-charging current fixed 50 mA
- Termination voltage 4.1V, 4.2V (default), 4.3V and 4.4V
- Restart level 50 mV, 100 mV (default), 150 mV and 200 mV below Termination voltage
- End of Charge 0.05C, 0.1C, 0.15C (default) and 0.2C
- Input voltage operating range 4.5 - 6.8V

REGULATORS

Eight low dropout linear regulators provide programmable voltage outputs with current capabilities of 80 mA, 150 mA, and 300 mA as given in the table below. LDO1 and LDO2 are supplied either by the VBATT (SEL=GND) or by buck regulator's output (SEL=VBATT). If the supply voltage is low (supply from buck), then LDO1 and LDO2 are going to be low-input low-output (LILO) LDOs.

Buck regulator can provide 700 mA (typ.) of current. If the buck is used for supplying LDO1 and LDO2 it won't be able to supply external devices. If LDO1 and LDO2 are supplied by VBATT, then buck can be used as an output power channel for digital loading with the default output voltage value of 1.8V

Under voltage lockout oversees device start up with a preset level of 3.0V(typ.).

Table 2. LDOs and Buck Default Voltages (for options LP3923TL/X and LP3923TL/X-VI)

Device	Type	Current (mA)	Enable control	Input	Output(V)	Startup default	Input	Output(V)	Startup default
				SEL=BATT			SEL=GND		
Buck		700	SI	VINB=BATT	2.0(1)	ON	VINB=BATT	1.8(1)	ON
LDO1	LILO	300	SI	VIN1=VBUCK	1.8	ON	VIN1=BATT	3	ON
LDO2	LILO	300	SI	VIN1=VBUCK	1.8	ON	VIN1=BATT	3	ON
LDO3	D	300	-	VIN2=BATT	3	ON	VIN2=BATT	3	ON
LDO4	A	80	TCXO_EN	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF
LDO5	A	150	RX_EN	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF
LDO6	A	150	TX_EN	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF
LDO7	A	150	SI	VIN2=BATT	3	ON	VIN2=BATT	3	ON
LDO8	D	150	SI	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF

(1) Voltage is set by the external resistors.

Table 3. LDOs and Buck Default Voltages (for options LP3923TL/X-VB and LP3923TL/X-VC)

Device	Type	Current (mA)	Enable control	Input	Output(V)	Startup default	Input	Output(V)	Startup default
				SEL=BATT			SEL=GND		
Buck		700	SI	VINB=BATT	2.0(1)	ON	VINB=BATT	1.8(1)	ON
LDO1	LILO	300	SI	VIN1=VBUCK	1.8	ON	VIN1=BATT	3	OFF
LDO2	LILO	300	SI	VIN1=VBUCK	1.8	ON	VIN1=BATT	3	OFF
LDO3	D	300	-	VIN2=BATT	3	ON	VIN2=BATT	3	ON
LDO4	A	80	TCXO_EN	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF
LDO5	A	150	RX_EN	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF
LDO6	A	150	TX_EN	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF
LDO7	A	150	SI	VIN2=BATT	3	ON	VIN2=BATT	3	ON
LDO8	D	150	SI	VIN2=BATT	3	OFF	VIN2=BATT	3	OFF

(1) Voltage is set by the external resistors.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

CHG_IN (V_{BATT}=2.8-5.5V)	−0.3V to +28V
V_{BATT}=VIN1-2, BATT, HF_PWR, VINB	−0.3V to +6.0V
All other inputs	−0.3V to V_{BATT}+0.3V, max 6.0V
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature	−40°C to +150°C
Max Continuous Power Dissipation(4) P_{D-MAX}(5)	Internally Limited
ESD(6)	
BATT, VIN1, VIN2, HF_PWR, CHG_IN, PWR_ON, VINB	8 kV HBM

(1) All voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Care must be exercised where high power dissipation is likely. The maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependant on the maximum operating junction temperature (TJ-MAX-OP), the maximum power dissipation of the device in the application (PD-MAX), and the junction to ambient thermal resistance of the package in the application (θJA). This relationship is given by the following equation: TA-MAX = TJ-MAX-OP - (θJA x PD-MAX)
(5) Internal Thermal Shutdown circuitry protects the device from permanent damage.
(6) The human-body model is 100 pF discharged through 1.5 kΩ. The machine model is a 200 pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

Operating Ratings(1)(2)

CHG_IN(3)	4.5 to 6.8V
V_{BATT} = VIN1-2, BATT, VINB	3.0V to 5.5V
HF_PWR, PWR_ON	0V to 5.5V
ACOK_N, SDA, SCL, RX_EN, TX_EN, TCXO_EN, PS_HOLD, RESET_N	0V to (V_{LDO} + 0.3V)
All other pins	0V to V_{BATT} + 0.3V)
Junction Temperature (T_J)	−40°C to +125°C
Ambient Temperature (T_A)(4)	−40°C to +85°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Full charging current is ensured for CHG_IN = 4.5 to 6.8V, but particularly at higher input voltages. Increased power dissipation may cause the thermal regulation to limit the current to a safe level, resulting in longer charging time.
(4) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Thermal Properties(5)

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Jedec Standard Thermal PCB)	
DSBGA 30	39°C/W

(5) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

General Electrical Characteristics

Unless otherwise noted, V_{IN} (= VIN1 = VIN2 = VINB = BATT) = 3.6V, GND = 0V, C_{VIN1-2} = C_{VINB} = 10 µF, C_{LDOx} = 1 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

General Electrical Characteristics (continued)

Unless otherwise noted, V_{IN} (= VIN1 = VIN2 = VINB = BATT) = 3.6V, GND = 0V, C_{VIN1-2} = C_{VINB} = 10 µF, C_{LDOx} = 1 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$I_{Q(STANDBY)}$	Standby Supply Current	V_{IN} = 3.6V, UVLO on, internal logic circuit on, all other circuits off.	2		**10**	µA
$I_{Q(SLEEP)}$	Sleep Mode Current @ 0 load	Buck, LDO1, LDO2, LDO3 and LDO7 enabled	130		**400**	µA
POWER MONITOR FUNCTIONS						
Battery Under-Voltage Lockout						
V_{UVLO-R}	Under Voltage Lock-out Rising	V_{IN} Rising	3.00	**2.85**	**3.15**	V
V_{UVLO-F}	Under Voltage Lock-out Falling	V_{IN} Falling (LP3923-VC)	2.80	**2.65**	**2.95**	
THERMAL SHUTDOWN						
	Higher Threshold	See(2)	160			°C
LOGIC AND CONTROL INPUTS						
V_{IL}	Input Low Level	PS_HOLD, SDA, SCL, RX_EN, TCXO_EN, TX_EN			**0.25* V_{LDO3}**	V
		PWR_ON, HF_PWR, SEL			**0.25* V_{BATT}**	V
V_{IH}	Input High Level	PS_HOLD, SDA, SCL, RX_EN, TCXO_EN, TX_EN		**0.75* V_{LDO3}**		V
		PWR_ON, HF_PWR, SEL		**0.75* V_{BATT}**		V
I_{IL}	Logic Input Current	All logic inputs except PWR_ON, HF_PWR. 0V ≤ V_{INPUT} ≤ V_{BATT}		**–5**	**+5**	µA
R_{IN}	Input Resistance	PWR_ON and HF_PWR Pull-Down resistance to GND(3)	500			kΩ
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output Low Level	PON_N, RESET_N, SDA, ACOK_N I_{OUT} = 2 mA			**0.25* V_{LDO3}**	V
V_{OH}	Output High Level	PON_N, RESET_N, ACOK_N I_{OUT} = −2 mA (Not applicable to Open Drain Output SDA)		**0.75* V_{LDO3}**		V

(2) Ensured by design.
(3) Ensured by design.

LDO1, LDO2 (LILO) Electrical Characteristics

Unless otherwise noted, if SEL=GND, then V_{IN}=VIN1=BATT=3.6V, if SEL=BATT, then V_{IN}=VIN1=VBUCK, GND = 0V, C_{VIN1-2} = 10 µF, C_{LDOx}= 1 µF. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1 mA, V_{OUT} = 3.0V		−2	+2	%
				−3	**+3**	
	Default Output Voltage	SEL = GND	3.0			V
		SEL = BATT	1.8			

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

LDO1, LDO2 (LILO) Electrical Characteristics (continued)

Unless otherwise noted, if SEL=GND, then V_{IN}=VIN1=BATT=3.6V, if SEL=BATT, then V_{IN}=VIN1=VBUCK, GND = 0V, C_{VIN1-2} = 10 µF, C_{LDOx}= 1 µF. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{OUT}	Output Current	$V_{INMIN} \le V_{IN} \le 5.5V$			**300**	mA
	Output Current Limit	V_{OUT} = 0V	600			
V_{DO}	Dropout Voltage	I_{OUT} =300 mA(2)(3)	135		180	mV
ΔV_{OUT}	Line Regulation	$V_{INMIN} \le V_{IN} \le 5.5V$ I_{OUT} = 1 mA	2			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 300 mA	5			
PSRR	Power Supply Ripple Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF, V_{OUT} = 3.0V, I_{OUT} = 20 mA(2)	60			dB
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 1 µF, I_{OUT} = 300 mA(2)	35			µs
$T_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT} = 300 mA(2)			**30**	mV

(2) Ensured by design.
(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

LDO3 (D-Type) Electrical Characteristics

Unless otherwise noted, V_{IN}=VIN2=BATT=3.6V, GND = 0V, C_{VIN1-2} = 10 µF, C_{LDOx}= 1 µF. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1 mA, V_{OUT} = 3.0V		−2	+2	%
				−3	**+3**	
	Default Output Voltage		3.0			V
I_{OUT}	Output Current	$V_{INMIN} \le V_{IN} \le 5.5V$			**300**	mA
	Output Current Limit	V_{OUT} = 0V	600			
V_{DO}	Dropout Voltage	I_{OUT} = 300 mA(2)(3)	135		250	mV
ΔV_{OUT}	Line Regulation	$V_{INMIN} \le V_{IN} \le 5.5V$ I_{OUT} = 1 mA	2			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 300 mA	5			
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF(2)	35			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF, I_{OUT} = 20 mA(2)	60			dB
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 1 µF, I_{OUT} = 300 mA(2)	35			µs
$T_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT} = 300 mA(2)			**30**	mV

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.
(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

LDO4 (A-Type) Electrical Characteristics

Unless otherwise noted, V_{IN}=VIN2=BATT=3.6V, GND = 0V, $C_{V!N1-2}$ = 10 µF, C_{LDOx}= 1 µF, TCXO_EN high. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1 mA, V_{OUT} = 3.0V		−2	+2	%
				−3	**+3**	
	Default Output Voltage		3.0			V
I_{OUT}	Output Current	$V_{INMIN} \le V_{IN} \le 5.5V$			**80**	mA
	Output Current Limit	V_{OUT} = 0V	400			
V_{DO}	Dropout Voltage	I_{OUT} =80 mA(2)(3)	60		85	mV
ΔV_{OUT}	Line Regulation	V_{INMIN} + ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1 mA	1			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 80 mA	5			
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF(2)	10			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF, I_{OUT} = 20 mA(2)	75			dB
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 1 µF, I_{OUT} = 80 mA(2)	35			µs
$T_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT} = 80 mA(2)			**30**	mV

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.
(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

LDO5, LDO6, LDO7 (A-Type) Electrical Characteristics

Unless otherwise noted, V_{IN}=VIN2=BATT=3.6V, GND = 0V, $C_{V!N1-2}$ = 10 µF, C_{LDOx}= 1 µF, RX_EN, TX_EN high. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1 mA, V_{OUT} = 3.0V		−2	+2	%
				−3	**+3**	
	Default Output Voltage		3.0			V
I_{OUT}	Output Current	$V_{INMIN} \le V_{IN} \le 5.5V$			**150**	mA
	Output Current Limit	V_{OUT} = 0V	400			
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA(2)(3)	100		150	mV
ΔV_{OUT}	Line Regulation	$V_{INMIN} \le V_{IN} \le 5.5V$, I_{OUT} = 1 mA	1			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 150 mA	5			
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF(2)	10			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF, I_{OUT} = 20 mA(2)	75			dB

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.
(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

LDO5, LDO6, LDO7 (A-Type) Electrical Characteristics (continued)

Unless otherwise noted, V_{IN}=VIN2=BATT=3.6V, GND = 0V, C_{VIN1-2} = 10 µF, C_{LDOx}= 1 µF, RX_EN, TX_EN high. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 1 µF, I_{OUT} = 150 mA(2)	35			µs
$T_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT} = 150 mA(2)			**30**	mV

LDO8 (D-Type) Electrical Characteristics

Unless otherwise noted, V_{IN}=VIN2=BATT=3.6V, GND = 0V, C_{VIN1-2} = 10 µF, C_{LDOx}= 1 µF. Note V_{INMIN} is the greater of 3.0V or V_{OUT} +0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1 mA, V_{OUT} = 3.0V		−2	+2	%
				−3	**+3**	
	Default Output Voltage		3.0			V
I_{OUT}	Output Current	V_{INMIN} ≤ V_{IN} ≤ 5.5V			**150**	mA
	Output Current Limit	V_{OUT} = 0V	400			
V_{DO}	Dropout Voltage	I_{OUT} = 150 mA(2)(3)	125		140	mV
ΔV_{OUT}	Line Regulation	V_{INMIN} ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1 mA	2			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ 150 mA	5			
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, C_{OUT} = 1 µF(2)	35			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	F = 10 kHz, C_{OUT} = 1 µF, I_{OUT} = 20 mA (2)	60			dB
$t_{START-UP}$	Start-Up Time from Shut-down	C_{OUT} = 1 µF, I_{OUT} = 150 mA(2)	35			µs
$T_{Transient}$	Start-Up Transient Overshoot	C_{OUT} = 1 µF, I_{OUT} = 150 mA(2)			**30**	mV

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.
(3) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

Buck Converter Electrical Characteristics

Unless otherwise noted, VIN = VINB = 3.6V, GND = 0V, C_{VINB} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_A = T_J = −40°C to +125°C.(1)(2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{FB}	Feedback Voltage (BUCK)	3.0V ≤V_{IN}≤ 5.5V	0.5	**0.485**	**0.515**	V
$V_{OUT,PWM}$	Output Voltage	3.0V ≤V_{IN}≤ 5.5V, I_{OUT} = 150mA External resistor divider accuracy not considered. R_{FB1}=390kΩ R_{FB2}=150kΩ(3)	1.8	**1.746**	**1.854**	V

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Buck output voltage accuracy depends on the accuracy of the external feedback resistors. Resistor values should be chosen for the divider network to ensure that at the desired output voltage the FB pin is at the specified value of 0.5V. See Buck Converter Application Information.
(3) Ensured by design.

Buck Converter Electrical Characteristics (continued)

Unless otherwise noted, VIN = VINB = 3.6V, GND = 0V, C_{VINB} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C.(1)(2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$V_{OUT,PFM}$	Output Voltage regulation in PFM mode relative to regulation in PWM mode	See(3)	1.5			%
V_{OUT}	Line Regulation	3.0V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 10 mA	0.14			%/V
	Load Regulation	100 mA ≤ I_{OUT} ≤ 300 mA	0.0013			%/mA
I_{LIM_PWM}	Switch Peak Current Limit	PWM Mode	1150	**800**	**1500**	mA
$R_{DSON(P)}$	P Channel FET on Resistance	V_{IN} = 3.6V I_{DS} = 100 mA	310			mΩ
$R_{DSON(N)}$	N Channel FET on Resistance		160			mΩ
f_{OSC}	Internal Oscillator Frequency	PWM Mode	2	1.9	2.1	MHz
Efficiency		I_{OUT} = 5 mA, PFM Mode V_{OUT} = 1.8V(3)	88			%
		I_{OUT} = 300 mA, PWM Mode V_{OUT} = 1.8V(3)	90			
T_{STUP}	Start Up Time	I_{OUT} = 0(3), V_{OUT} = 1.8V	140			µs

Charger Electrical Characteristics

Unless otherwise noted, V_{CHG_IN} = 5V, V_{IN}= BATT = 3.6V, C_{CHG_IN} = 1 µF, V_{BATT} = 30 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −25°C to +85°C.(1)(2)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{CHG_IN}	AC wall adapter input voltage operating range			**4.5**	**6.8**	V
V_{OK_CHG}	CHG_IN OK trip-point.	V_{CHG_IN} - V_{BATT} (Rising)	150			mV
		V_{CHG_IN} - V_{BATT} (Falling)	40			
V_{TERM}	Battery charging termination voltage tolerance	V_{TERM} = 4.2V, I_{CHG} = 50 mA V_{TERM} is measured at 10% of the programmed I_{CHG} current		-0.35 **-1**	+0.35 **+1**	%
I_{CHG}	CHG_IN programmable full-rate charging current	6.8V ≥ V_{CHG_IN} ≥ 4.5V V_{BATT} < V_{CHG_IN} − V_{OK_CHG} V_{FULL_RATE} < V_{BATT} < V_{TERM}(3)		**50**	**1200**	mA
	Full rate charging current tolerance	I_{CHG} = 400 mA		**−10**	**+10**	%
$I_{PREEQUAL}$	Pre-charging current	2.2V < V_{BATT} < V_{FULL_RATE}	50	**30**	**70**	mA
V_{FULL_RATE}	Full-rate qualification threshold	V_{BATT} rising, transition from pre-charging to full-rate charging	2.8	**2.7**	**2.9**	V
		V_{BATT} rising, transition from pre-charging to full-rate charging (LP3923-VC)	3.0	**2.9**	**3.1**	

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(3) Full charging current is ensured for CHG_IN = 4.5 to 6.8V, but particularly at higher input voltages. Increased power dissipation may cause the thermal regulation to limit the current to a safe level, resulting in longer charging time.

Charger Electrical Characteristics (continued)

Unless otherwise noted, V_{CHG_IN} = 5V, V_{IN}= BATT = 3.6V, C_{CHG_IN} = 1 µF, V_{BATT} = 30 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −25°C to +85°C.(1)(2)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{EOC}	End-of-charging current, % of full-rate current	0.1C option selected	10			%
$V_{RESTART}$	Restart threshold voltage	From V_{TERM} voltage (4.2V, −100 mV options selected)	−100	**−70**	**−130**	mV
I_{MON}	I_{MON} Voltage 1	I_{CHG} = 100 mA	0.247			V
	I_{MON} Voltage 2	I_{CHG} = 400 mA	0.988	0.840	1.127	
C_{BATT}	Capacitance on BATT	See(4)		**30**	**1000**	µF
T_{REG}	Regulated junction temperature	See(4)	115			°C
Detection and Timing (one combined timer)						
T_{POK}	Power OK deglitch time	$V_{CHG} > V_{BATT} + V_{OK\_CHG}$	30			ms
T_{PC_FULL}	Deglitch time	From pre-charging to full-rate charging	210			ms
T_{CHG}	Charge timer	Pre-charge mode	1			Hrs
		CC mode/CV mode (combined timer)	disabled			
			2			
			5			
			8			
T_{EOC}	Deglitch time for end- of-charge transition		210			ms

(4) Ensured by design.

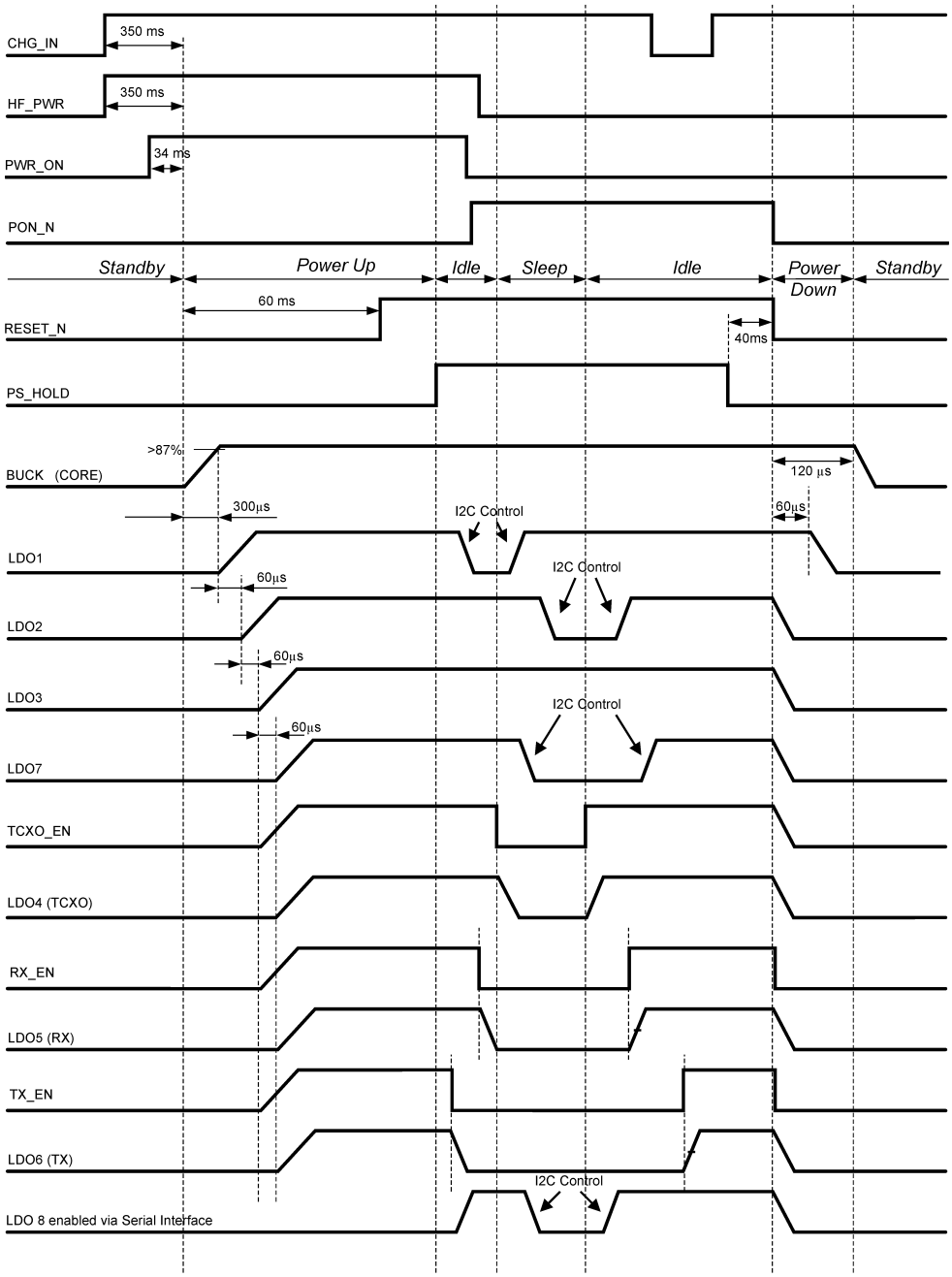
Serial Interface

Unless otherwise noted, V_{IN} = BATT = 3.6V, GND = 0V, $C_{VIN1–2}$ = 10 µF C_{LDOx} = 1 µF and V_{LDO3} = 3.0V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_A = T_J$ = −40°C to +125°C.(1)(2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
f_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time between START and STOP			1.3		µs
t_{HOLD}	Hold Time Repeated START Condition			0.6		µs
t_{CLK-LP}	CLK Low Period			1.3		µs
t_{CLK-HP}	CLK High Period			0.6		µs
t_{SU}	Set-Up Time Repeated START Condition			0.6		µs
$t_{DATA-HOLD}$	Data Hold Time			50		ns
$t_{DATA-SU}$	Data Set-Up Time			100		ns
t_{SU}	Set-Up Time for STOP Condition			0.6		µs
t_{TRANS}	Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA & CLK Signals		50			ns

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.

POWER UP AND POWER DOWN SEQUENCES



(1) CHG_IN is edge sensitive and HF_PWR is level sensitive at startup in STANDBY mode and level sensitive in POWER-ON-RESET mode.

(2) PWR_ON is level sensitive at startup. PS_HOLD must be asserted before PWR_ON goes LOW to keep PMU powered. PWR_ON input is not monitored after PMU is powered up (PS_HOLD asserted).

(3) PON_N is a direct inversion of PWR_ON input when LDO3 is powered up (no power-on switch debouncing on PON_N output).

(4) The input signal which activates Power Up sequence (either PWR_ON or CHG_IN or HF_PWR) must be on when PS_HOLD is asserted.

(5) Time delay between the PS_HOLD going low and the start of Power Down sequence depends on PS_HOLD_DELAY setting (0=35ms, 1=350ms) (typ.).

Figure 1. Power Up and Power Down Timing Diagram

LP3923 Serial Port Communication: Slave Address Code: 7h'7E

Table 4. Control Registers(1)

Addr	Register (Default value)*	D7	D6	D5	D4	D3	D2	D1	D0
8h'00	OP_EN1 (01000111)	BUCK_ PWM	EN_ BUCK	X	X	EN_LDO8	EN_LDO7	EN_LDO2	EN_LDO1
8h'01	LDO1PGM O/P SEL=BATT (00001100) SEL=GND (00011011)	X	X	X	LDO1_ V1_OP[4]	LDO1_ V1_OP[3]	LDO1_ V1_OP[2]	LDO1_ V1_OP[1]	LDO1_ V1_OP[0]
8h'02	LDO2 Program O/P SEL=BATT (00001100) SEL=GND (00011011)	X	X	X	LDO2_ V2_OP[4]	LDO2_ V2_OP[3]	LDO2_ V2_OP[2]	LDO2_ V2_OP[1]	LDO2_ V2_OP[0]
8h'03	LDO3 PGM O/P (00011011)	X	X	X	LDO3_ V3_OP[4]	LDO3_ V3_OP[3]	LDO3_ V3_OP[2]	LDO3_ V3_OP[1]	LDO3_ V3_OP[0]
8h'04	LDO4 PGM O/P (00011011)	X	X	X	LDO4_ V4_OP[4]	LDO4_ V4_OP[3]	LDO4_ V4_OP[2]	LDO4_ V4_OP[1]	LDO4_ V4_OP[0]
8h'05	LDO5 PGM O/P (00011011)	X	X	X	LDO5_ V5_OP[4]	LDO5_ V5_OP[3]	LDO5_ V5_OP[2]	LDO5_ V5_OP[1]	LDO5_ V5_OP[0]
8h'06	LDO6 PGM O/P (00011011)	X	X	X	LDO6_ V6_OP[4]	LDO6_ V6_OP[3]	LDO6_ V6_OP[2]	LDO6_ V6_OP[1]	LDO6_ V6_OP[0]
8h'07	LDO7 PGM O/P (00011011)	X	X	X	LDO7_ V7_OP[4]	LDO7_ V7_OP[3]	LDO7_ V7_OP[2]	LDO7_ V7_OP[1]	LDO7_ V7_OP[0]
8h'08	LDO8 PGM O/P (00011011)	X	X	X	LDO8_ V8_OP[4]	LDO8_ V8_OP[3]	LDO8_ V8_OP[2]	LDO8_ V8_OP[1]	LDO8_ V8_OP[0]
8h'0C	Status1 Trig.-PWR_ON(10000010) Trig.-HF_PWR(01000010) Trig.-CHG_IN (00100010)	**PWR_ON TRIG**	**HF_PWR TRIG**	**CHG_IN TRIG**	**X**	**TSD_H**	**TSD_L**	**FF**	**X**
8h'10	CHARGER Control 1 (00010 001)	X	X	Force_ EOC	PROG_ CHGTIME[1]	PROG_ CHGTIME[0]	EN_EOC	X	EN_CHG
8h'11	CHARGER Control 2 (00000111)	X	X	X	PROG_ ICHG[4]	PROG_ ICHG[3]	PROG_ ICHG[2]	PROG_ ICHG[1]	PROG_ ICHG[0]
8h'12	CHARGER Control 3 (00011001)	X	X	VTERM[1]	VTERM[0]	PROG_ EOC[1]	PROG_ EOC[0]	PROG_ VSTRT[1]	PROG_ VSTART[0]
8h'13	CHARGER Status 1 (0000 0000)	**BATT_ OVER_OUT**	**CHGIN_ OK_OUT**	**EOC**	**TOUT_ FULLRATE**	**TOUT_ PRECHG**	**X**	**FULLRATE**	**PRECHG**
8h'14	CHARGER Status 2 (00000000)	X	X	X	X	X	X	**TOUT_ CONSTV**	**BAD_BATT**
8h'1C	MISC Control1 (00000000)	X	X	X	X	X	X	EN_ APU_TSD	PS_HOLD_ DELAY

(1) X — Not used.
BOLD locations are Read Only type.
NOTE: All Control registers apart from Charger Control registers (h'10 — h'12) are reset to default at the end of every Power Down sequence.

Table 5. Register 0x00 – OP_EN1

BUCK_PWM	0 - Auto mode PFM/PWM 1 - Buck forced PWM mode
EN_BUCK	0 - disable Buck 1 - enable Buck
EN_LDO8	0 - disable LDO8 1 - enable LDO8
EN_LDO7	0 - disable LDO7 1 - enable LDO7
EN_LDO2	0 - disable LDO2 on LP3923TL/X and -VI; enable on LP3923TL/X-VB 1 - enable LDO2 on LP3923TL/X and -VI; disable on LP3923TL/X-VB
EN_LDO1	0 - disable LDO1 on LP3923TL/X and -VI; enable on LP3923TL/X-VB 1 - enable LDO1 on LP3923TL/X and -VI; disable on LP3923TL/X-VB

Table 6. Register 0x0C (Read Only) – Status 1

PWR_ON_TRIG	0 - system was not powered on by PWR_ON input 1 - system was powered on by PWR_ON input
HF_PWR_TRIG	0 - system was not powered on by HF_PWR input 1 - system was powered on by HF_PWR input
CHG_IN_TRIG	0 - system was not powered on by connecting AC adapter 1 - system was powered on by connecting AC adapter
TSD_H	0 - Thermal Shutdown threshold not exceeded 1 - Thermal Shutdown threshold exceeded (cause Power Down sequence)
TSD_L	0 - chip temperature has not been over TSD early warning threshold 1 - chip temperature has been over TSD early warning threshold
FF	0 - Buck output voltage out of range 1 - Buck output voltage within range

Table 7. Register 0x13 (Read Only) – CHARGER Status 1

BATT_OVER_OUT	0 - battery voltage is in normal range 1- battery voltage is over critical limit
CHGIN_OK_OUT	0 - voltage is not connected to AC adapter input 1 - voltage is connected to AC adapter input
EOC	0 - charging current is above EOC current level 1 - charging current is below EOC current level
TOUT_FULLRATE	0 - no time out occurred in Constant Current mode 1 - time out occurred in Constant Current mode
TOUT_PRECHG	0 - no time out occurred in pre-charge mode 1 - time out occurred in pre-charge mode
FULLRATE	0 - charger is not in CC or CV mode 1 - charger is in CC or CV mode
PRECHG	0 - charger is not in pre-charge mode 1 - charger is in pre-charge mode

Table 8. Register 0x14 (Read Only) – CHARGER Status 2

TOUT_CONSTV	0 - no time out occurred in Constant Voltage mode 1 - time out occurred in Constant Voltage mode
BAD_BATT	0 - charger has not detected a bad battery 1 - charger has detected a bad battery

Table 9. Register 0x1C – MISC Control 1

EN_APU_TSD	0 - do not start PMU automatically after TSD event
	1 - start PMU automatically after TSD event
PS_HOLD_DELAY	0 - PMU powerdown after PS_HOLD has been low for 35 ms
	1 - PMU powerdown after PS_HOLD has been low for 350 ms

LDO OUTPUT VOLTAGE PROGRAMMING

The following table summarizes the supported output voltages for LP3923. Default voltages after start-up sequences have been highlighted in **bold.**

Data Code LDO_Vx_OP[x]	LDOx [V]	Data Code LDO_Vx_OP[x]	LDOx [V]
8h'00	1.20	8h'10	2.20
8h'01	1.25	8h'11	2.40
8h'02	1.30	8h'12	2.50
8h'03	1.35	8h'13	2.60
8h'04	1.40	8h'14	2.65
8h'05	1.45	8h'15	2.70
8h'06	1.50	8h'16	2.75
8h'07	1.55	8h'17	2.80
8h08	1.60	8h'18	2.85
8h'09	1.65	8h'19	2.90
8h'0A	1.70	8h'1A	2.95
8h'0B	1.75	8h'1B	**3.00** (1)
8h'0C	**1.80** (1)	8h'1C	3.05
8h'0D	1.85	8h'1D	3.10
8h'0E	1.90	8h'1E	3.20
8h'0F	2.00	8h'1F	3.3

(1) See Table 1.

CHARGING CURRENT PROGRAMMING

Table 10. The following table summarizes the supported currents for LP3923.

PROG_ ICHG[4]	PROG_ ICHG[3]	PROG_ ICHG[2]	PROG_ ICHG[1]	PROG_ ICHG[0]	ICHG (mA)
0	0	0	0	0	50
0	0	0	0	1	100
0	0	0	1	0	150
0	0	0	1	1	200
0	0	1	0	0	250
0	0	1	0	1	300
0	0	1	1	0	350
0	0	1	1	1	**400 (Default)**
0	1	0	0	0	450
0	1	0	0	1	500
0	1	0	1	0	550
0	1	0	1	1	600
0	1	1	0	0	650
0	1	1	0	1	700
0	1	1	1	0	750
0	1	1	1	1	800
1	0	0	0	0	850

Table 10. The following table summarizes the supported currents for LP3923. (continued)

PROG_ ICHG[4]	PROG_ ICHG[3]	PROG_ ICHG[2]	PROG_ ICHG[1]	PROG_ ICHG[0]	ICHG (mA)
1	0	0	0	1	900
1	0	0	1	0	950
1	0	0	1	1	1000
1	0	1	0	0	1050
1	0	1	0	1	1100
1	0	1	1	0	1150
1	0	1	1	1	1200

Table 11. Charging Termination Voltage Programming

VTERM[1]	VTERM[0]	V_{TERM}
0	0	4.1
0	**1**	**4.2 (Default)**
1	0	4.3
1	1	4.4

Table 12. End of Charging Current Programming

PROG_EOC[1]	PROG_EOC[0]	I_{EOC} (1)
0	0	0.05C
0	1	0.1C
1	**0**	**0.15C (Default)**
1	1	0.2C

(1) C is the programmed charging current.

Table 13. Charging Restart Voltage Programming

PROG_VRSTRT[1]	PROG_VRSTRT[0]	Restart Voltage (V)
0	0	V_{TERM} −50 mV
0	**1**	**V_{TERM} −100 mV (Default)**
1	0	V_{TERM} −150 mV
1	1	V_{TERM} −200 mV

Table 14. Charge Timer Programming

PROG_CHGTIME[1]	PROG_CHGTIME[0]	Charging Timer (Hrs)
0	0	Disabled
0	1	2
1	**0**	**5 (Default)**
1	1	8

BATTERY CHARGE MANAGEMENT

A charge management system allowing safe charge and maintenance of a Li-Ion battery is implemented on the LP3923. It has a CC/CV linear charge capability with programmable battery regulation voltage and end of charging current threshold. A maintenance mode utilizing programmable restart voltage levels enables the battery voltage to be maintained at the correct level. The charging current in the constant voltage mode is programmable from 50 mA to 1.2A in 50 mA steps.

If PMU is started without a battery, and the battery is attached later, the charging current should be programmed once more; otherwise, the charging current will be the same as without a battery.

If the battery is deeply depleted and the overdischarge protection circuit is active, during startup the charger may detect that the battery is not present. This can cause the charger to select a non-default charging current (LDO mode default charging current).

CHARGER FUNCTION

Following the correct detection of an input voltage at the charger pin the charger enters a pre-charge mode. In this mode a constant current of 50 mA is available to charge the battery to 2.8V. At this voltage level the charge management applies the full rate constant current to raise the battery voltage to the termination voltage level (default 4.2V). The full-rate charging current may be programmed to a different level at this stage. When termination voltage (VTERM) is reached, the charger is in constant voltage mode and a constant voltage of 4.2V is maintained. This mode is complete when the end of charging current (default 0.15C) is detected and the charge management enters the maintenance mode. In maintenance mode the battery voltage is monitored for the restart level (default VTERM - 100 mV) and the charge cycle is re-initiated to re-establish the termination voltage level.

THERMAL SHUTDOWN

The Thermal Shutdown (TSD) function monitors the chip temperature to protect the chip from temperature damage caused, for example, by excessive power dissipation. If the temperature exceeds a higher threshold value of +160°C, the TSD_H bit in the Register 0x0C is set, and the chip will automatically run the Power Down sequence.

The restart operation after Thermal Shutdown can be initiated only after the chip has cooled down to the +90°C threshold. The APU_TSD_EN bit in the Register 0x1C is controlling the restart. If this bit is cleared (default) then a Power On sequence is initiated normally through PWR_ON, CHG_IN or VBUS. If APU_TSD_EN is written to logic 1 then an automatic Power Up sequence is initiated. All register settings preserved in such case. Power On can be activated only if the junction temperature is less than the early warning lower threshold +90°C.

The temperature monitoring function has two charger threshold values that result in protective actions. When a lower threshold of +105°C is exceeded, the TSD_L bit in Register 0x0C will be set, bit will reset it if the temperature has decreased to lower than 15°C below the threshold.

When a upper charger threshold of +115°C is exceeded, the charger will reduce charging current to protect the chip.

Parameter	Typ	Unit
Higher Threshold(1)	160	°C
Charger Early Warning(1)	105	°C
Early Warning Hysteresis(1)	15	°C
Charger Thermal Regulation	115	°C

(1) Ensured by design.

TERMINATION AND RESTART

The termination and restart voltage levels are determined by the data in the VTERM[1:0] and PROG_VSTRT[1:0] bits in the control register. The restart voltage is programmed relative to the selected termination voltage.

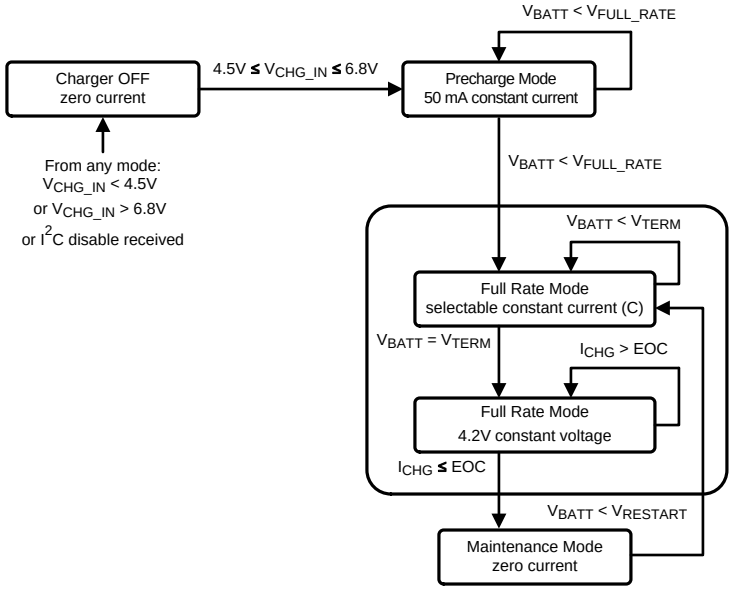


Figure 2. Simplified Charger Functional State Diagram (when EOC is enabled)

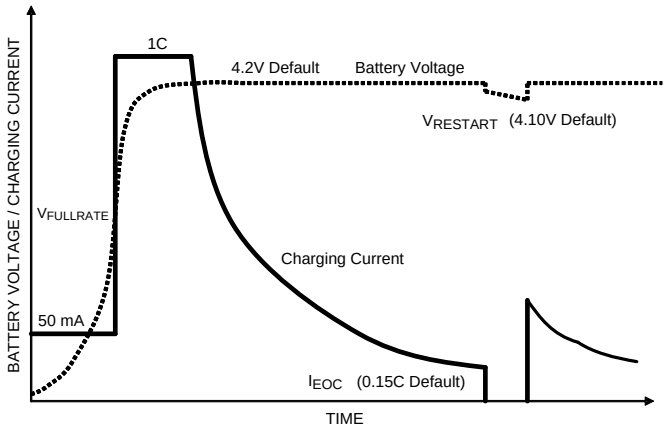


Figure 3. Charging Cycle Diagram

IMON CHARGING CURRENT MONITOR

Charging current is monitored within the charger section and a proportional voltage representation of the charging current is presented at the IMON output pin. The output voltage relationship to the actual charging current is represented in the following graph and by the equation:

$$V_{IMON}(mV) = (2.47 \times I_{CHG}(mA)) \quad (1)$$

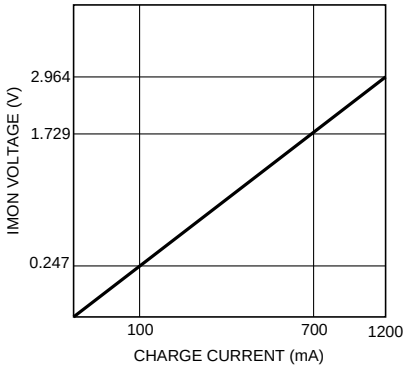


Figure 4.

Note that this function is not available if there is no input at CHG_IN or if the charger is off due to the input at CHG_IN being less than the compliance voltage.

Buck Converter Application Information

BUCK OUTPUT VOLTAGE SELECTION

Buck output voltage can be programmed via the selection of the external feedback resistor network forming the output feedback between the output voltage side of the inductor and the FB pin and the FB pin and GND.

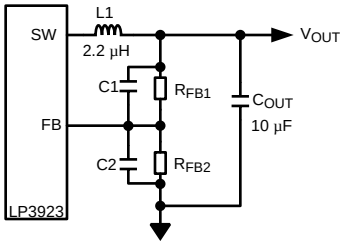


Figure 5. Buck Converter Components

V_{OUT} will be adjusted to make the voltage at FB equal to 0.5V. The resistor from FB to ground (R_{FB2}) should be around 200 kΩ to keep the current drawn through the resistor network to a minimum but large enough that it is not susceptible to noise. If R2 is 200 kΩ and with V_{FB} at 0.5V, the current through the resistor feedback network will be 2.5 µA.

The formula for output voltage selection is

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (2)$$

V_{OUT} - output voltage (V)

V_{FB} - feedback voltage (0.5V)

R_{FB1} - feedback resistor from V_{OUT} to FB

R_{FB2} - feedback resistor from FB to GND

The recommended value for C1 is 2.2 pF to 5.1 pF, and for C2 is 15 pF.

Table 15. Component Configurations for Various Output Voltage Values

V_{OUT} [V]	R_{FB1} [kΩ]	R_{FB2} [kΩ]	C1 [pF]	C2 [pF]	L [µH]	C_{OUT} [µF]
1.4	360	200	2.2 to 5.1	15	2.2	10
1.6	390	178	2.2 to 5.1	15	2.2	10
1.8	390	150	2.2 to 5.1	15	2.2	10
2.0	453	150	2.2 to 5.1	15	2.2	10

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically given at 25°C so ratings at the application maximum ambient temperature should be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating.

Method 1

The total current is the sum of the load and the inductor ripple current. This can be written as:

$$I_{SAT} = I_{OUTMAX} + I_{RIPPLE}$$

$$I_{SAT} = I_{OUTMAX} + \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right) \quad (3)$$

I_{LOAD} = load current

I_{RIPPLE} = average to peak inductor current

V_{IN} = input voltage

L = inductor inductance

f = switching frequency

Method 2

A more conservative approach is to choose an inductor that can handle the maximum current limit of 1500 mA. Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least:

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) x \left(\frac{V_{OUT}}{V_{IN} x f}\right) \quad (4)$$

A 2.2 µH inductor with a saturation current rating of at least 1500 mA is recommended for most applications. The inductor's resistance should be less than 0.3Ω for good efficiency. The below table suggests inductors and suppliers.

For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

Table 16. Suggested Inductors and Their Suppliers (Preliminary and Untested)

Model	Vendor	Dimensions (mm)	DC R(max)
DO3314-222MXC	Coilcraft	3.3 x 3.3 x 1.4	200 mΩ
LPO3310-222MX	Coilcraft	3.3 x 3.3 x 1.0	150 mΩ
ELL5GM2R2N	Panasonic	5.2 x 5.2 x x 1.5	53 mΩ
CDRH2D142R2	Sumida	3.2 x 3.2 x 1.55	94 mΩ

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 10 µF is sufficient for most applications. A larger value may be used for improved input voltage filtering. Use X7R or X5R type capacitors, do not use Y5V. The DC bias characteristics of ceramic capacitors must be considered when selecting case sizes of 0805 or smaller for use in the application. Smaller case sizes in many cases exhibit a large drop in capacitance value as the DC bias increases.

The input filter capacitor supplies current to the PFET switch of the converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with a surge current rating sufficient for the power-up surge from the input power source. The power-up surge current is approximately the capacitor's value (µF) times the voltage rise rate (V/µs).

The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} x \sqrt{\frac{V_{OUT}}{V_{IN}} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst case I_{RMS} is:

$$I_{RMS} = \frac{I_{OUTMAX}}{2} \text{ (duty cycle = 50\%)} \quad (6)$$

OUTPUT CAPACITOR SELECTION

A 10 µF capacitor is recommended for use at the output of the buck converter. Use X7R or X5R type capacitors; do not use Y5V. The DC bias characteristics of ceramic capacitors must be considered when selecting case sizes of 0805 or smaller for use in the application. Smaller case sizes in many cases exhibit a large drop in capacitance value as the DC bias increases. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR. It can be calculated as:

Voltage peak to peak ripple due to capacitance =

$$V_{PP\text{-}C} = \frac{I_{PP}}{f \times 8 \times C} \quad (7)$$

Voltage peak to peak ripple due to ESR =

$$V_{PP\text{-}ESR} = I_{PP} * R_{ESR} \quad (8)$$

Voltage peak to peak ripple, root mean squared =

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2} \quad (9)$$

Note that the output ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). Because these two components are out of phase the rms value is used. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the frequency of the R_{ESR} given is the same order of magnitude as the switching frequency.

Table 17. Suggested Capacitors And Their Suppliers

Model	Type	Vendor	Voltage Rating	Case Size
10 µF (C_{IN} and C_{OUT})				
GRM21BR60J106k	**Ceramic, X5R**	**MURATA**	**6.3V**	**0805**
JMK212BJ106K	**Ceramic, X5R**	**TAIYO YUDEN**	**6.3V**	**0805**
C2012X5R0J106K	**Ceramic, X5R**	**TDK**	**6.3V**	**0805**

LDO Information

OPERATIONAL INFORMATION

The LP3923 has eight LDOs of which 4 are enabled by default and powered up during the power up sequence, LDOs 1, 2, 3 and 7 are powered up during the power up sequence. LDOs 4, 5, and 6 are separately externally enabled and will follow LDO3 in start up if their respective enable pin is pulled high. LDO1, LDO2, LDO7 and LDO8 can be enabled/disabled via the Serial Interface

LDO3 must remain in regulation otherwise the device will power down.

The LILO-type LDO is optimized for low output voltage and for good dynamic performance to supply different fast charging (digital) pads.

INPUT VOLTAGES

There are two input voltage pins used to power the eight LDOs on the LP3923. V_{IN1} is the supply for LDO1 and LDO2. V_{IN2} is the supply for LDO3, LDO4, LDO5, LDO6, LDO7, and LDO8.

EXTERNAL CAPACITORS

The Low Drop Out Linear Voltage regulators on the LP3923 require external capacitors to ensure stable outputs. The LDOs on the LP3923 are specifically designed to use small surface mount ceramic capacitors which require minimum board space. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

Input capacitors are required for correct operation. It is recommended that a 10 µF capacitor be connected between each of the voltage input pins and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. A ceramic capacitor is recommended although a good quality tantalum or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain within its operational range over the entire operating temperature range and conditions.

OUTPUT CAPACITOR

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC-bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value.

The LP3923 is designed specifically to work with very small ceramic output capacitors. The LDOs on the LP3923 are specifically designed to be used with X7R and X5R type capacitors. With these capacitors, selection of the capacitor for the application is dependant on the range of operating conditions and temperature range for that application. (See section on CAPACITOR CHARACTERISTICS).

It is also recommended that the output capacitor be placed within 1 cm from the output pin and returned to a clean ground line.

CAPACITOR CHARACTERISTICS

The LDOs on the LP3923 are designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around 1µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular, to ensure stability, the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

As an example Figure 6 shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

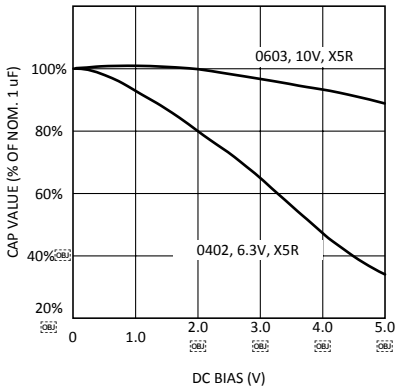


Figure 6. Graph Showing A Typical Variation in Capacitance vs DC Bias

Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 µF ceramic capacitor is in the range of 10 mΩ to 40 mΩ, and also meets the ESR requirement for stability.

The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range –55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of –55°C to +85°C. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from +25°C to +85°C. Therefore X7R is recommended over these other capacitor types in applications where the temperature will change significantly above or below +25°C.

No-Load Stability

The LDOs on the LP3923 will remain stable and in regulation with no external load.

LDO Output Capacitors, Recommended Specification(1)

Symbol	Parameter	Type	Typ	Min	Max	Units
C_O(LDO1)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO2)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO3)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO4)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO5)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO6)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO7)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF
C_O(LDO8)	Capacitance	X5R, X7R	1.0	**0.7**	**2.2**	µF

(1) The capacitor tolerance should be 30% or better over the full temperature range. X7R, or X5R capacitors should be used. These specifications are given to ensure stability of the supply outputs and care must be taken to ensure that the capacitance remains within these values over all conditions within the application. See Capacitor Characteristics section in Application Information.

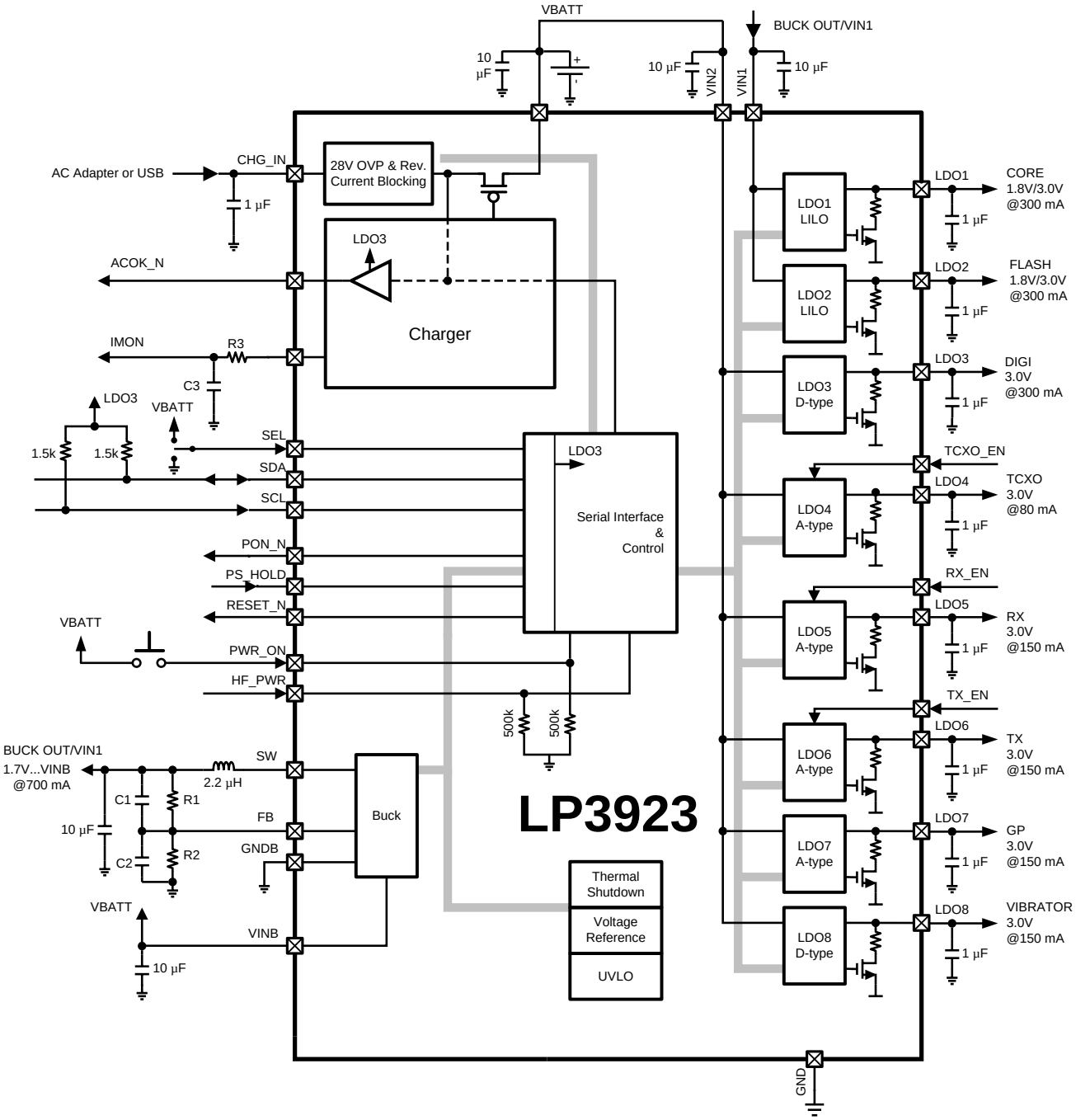


Figure 7. Typical Application Circuit
(Buck Output used as input for LILOs)

I²C Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 kΩ, and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

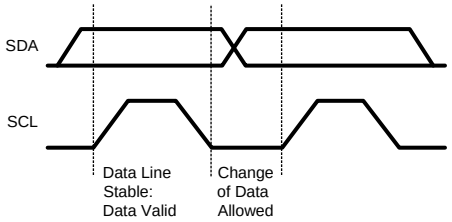


Figure 8. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

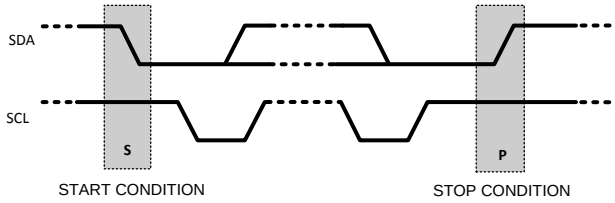


Figure 9. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

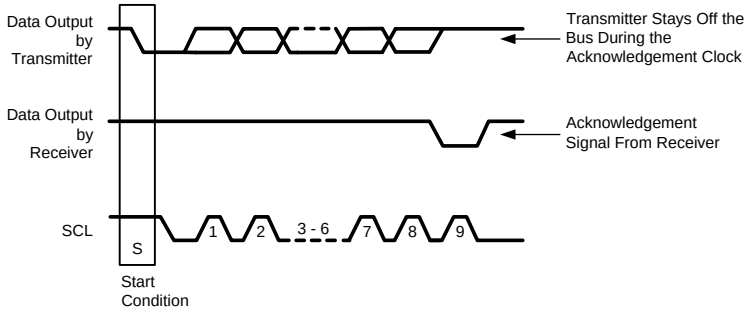


Figure 10. Bus Acknowledge Cycle

"ACKNOWLEDGE AFTER EVERY BYTE" RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP3923 operates as a slave device with the address 7h'7E (binary nnnnnnnn). Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

CONTROL REGISTER WRITE CYCLE

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

CONTROL REGISTER READ CYCLE

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.

- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = “1”).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

	Address Mode(1)
Data Read	<Start Condition> <Slave Address><r/w = ‘0’>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = ‘1’>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = ‘0’>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>

(1) < > Data from master [ ] Data from slave

REGISTER READ AND WRITE DETAIL

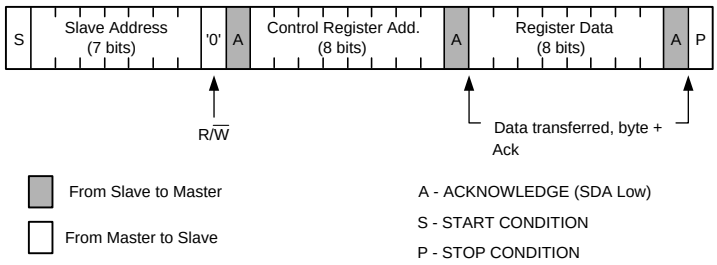


Figure 11. Register Write Format

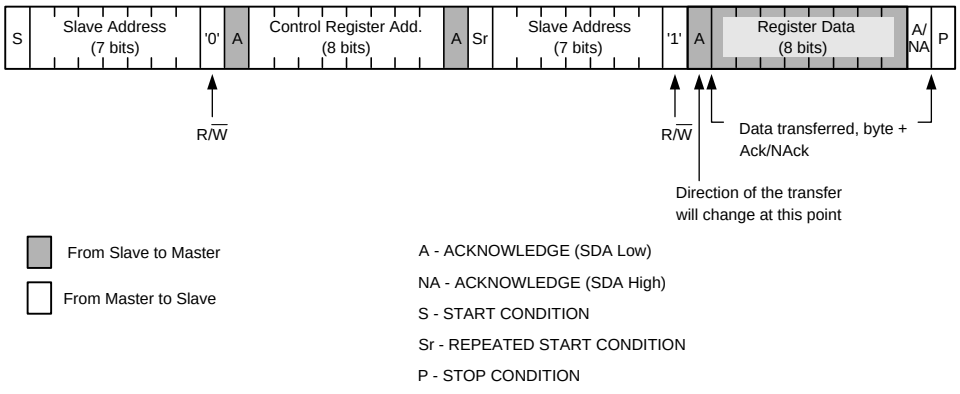


Figure 12. Register Read Format

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	30

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3923TL-VB/NOPB	NRND	DSBGA	YZR	30	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V020	
LP3923TL-VI/NOPB	NRND	DSBGA	YZR	30	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V017	
LP3923TL/NOPB	NRND	DSBGA	YZR	30	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3923	
LP3923TLX/NOPB	NRND	DSBGA	YZR	30	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3923	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

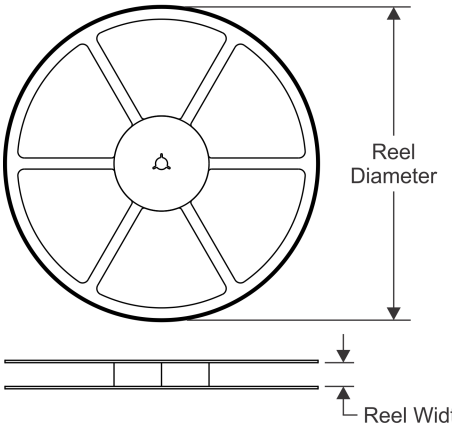
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

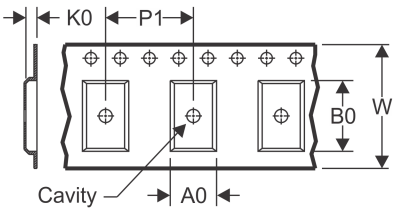
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

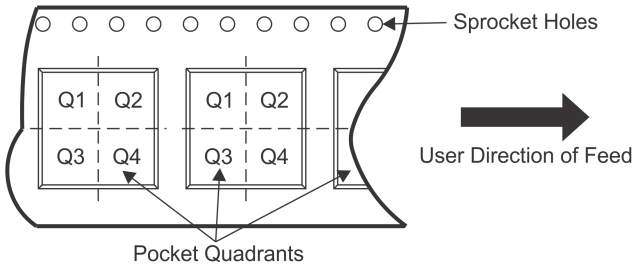


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

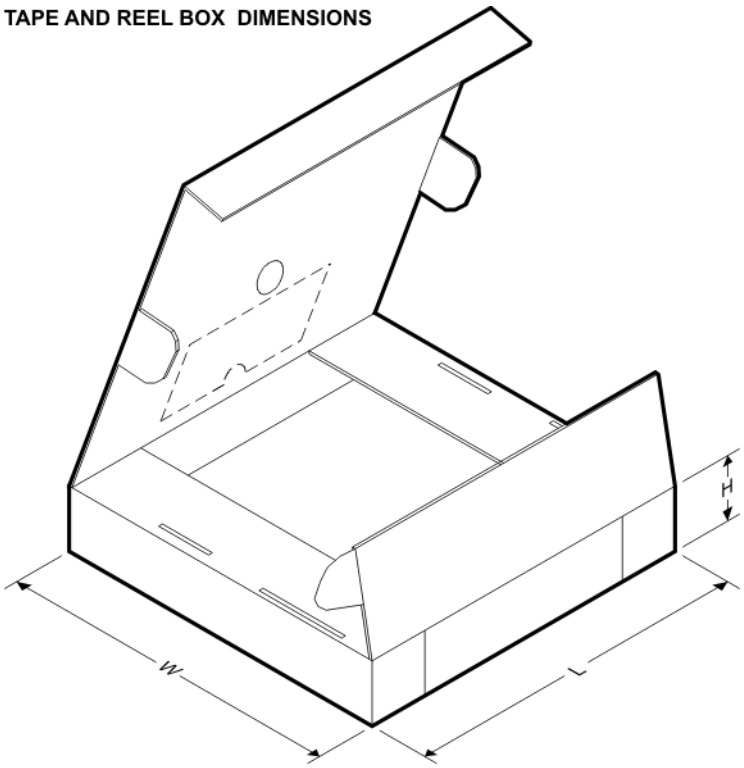
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3923TL-VB/NOPB	DSBGA	YZR	30	250	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1
LP3923TL-VI/NOPB	DSBGA	YZR	30	250	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1
LP3923TL/NOPB	DSBGA	YZR	30	250	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1
LP3923TLX/NOPB	DSBGA	YZR	30	3000	178.0	8.4	2.74	3.15	0.76	4.0	8.0	Q1

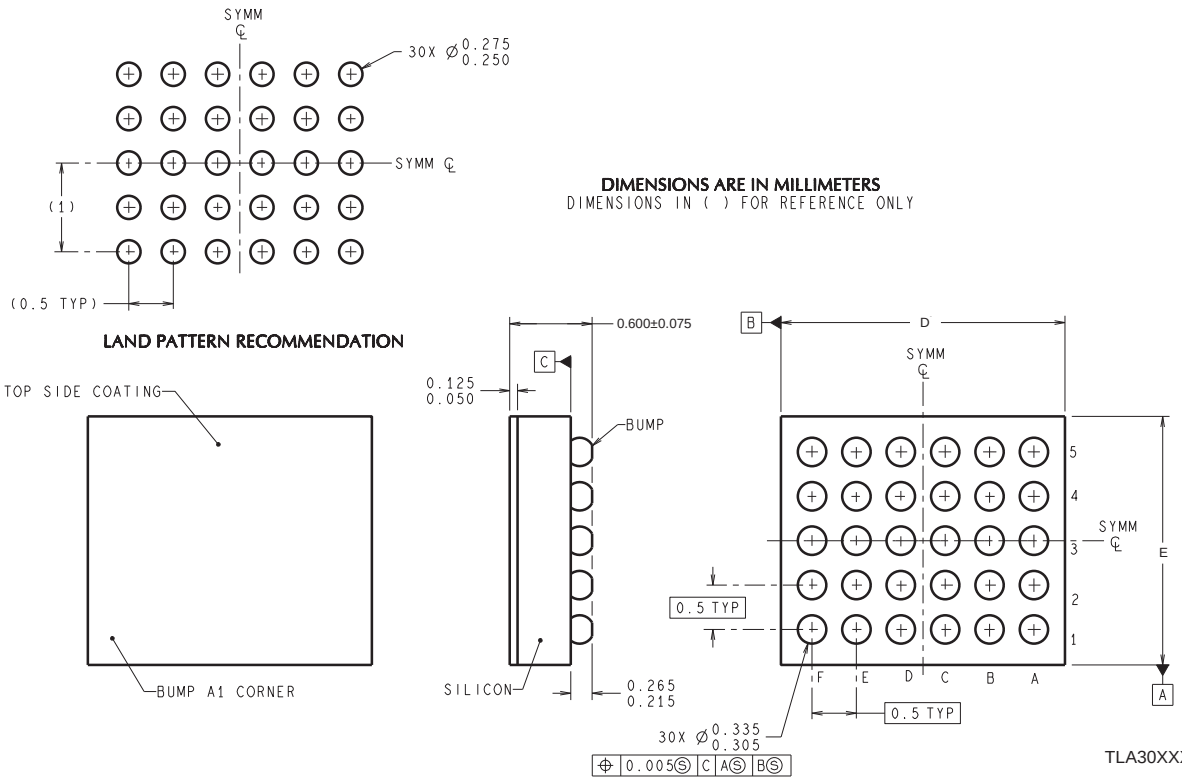
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3923TL-VB/NOPB	DSBGA	YZR	30	250	210.0	185.0	35.0
LP3923TL-VI/NOPB	DSBGA	YZR	30	250	210.0	185.0	35.0
LP3923TL/NOPB	DSBGA	YZR	30	250	210.0	185.0	35.0
LP3923TLX/NOPB	DSBGA	YZR	30	3000	210.0	185.0	35.0

YZR0030



D: Max = 2.99 mm, Min = 2.93 mm

E: Max = 2.49 mm, Min = 2.43 mm

4215057/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265