Click here to ask about the production status of specific part numbers.

MAX22005

12-Channel Factory-Calibrated Configurable Industrial-Analog Input

General Description

The MAX22005 is a twelve-channel industrial-grade analog input voltage-mode device that can also be configured as analog-input current-mode device using an external precision resistor per channel. It can also operate as configurable analog-input using an external precision resistor and low-cost switch per channel. Input channels can be used as twelve single-ended inputs, or six differential inputs, or up to eight multichannel configurable differential inputs. In total, the device supports up to 26 different configurations.

The MAX22005 features an integrated 24-bit delta-sigma ADC that is shared between all channels. The ADC can be used with either an integrated 5ppm/°C precision reference or an external reference. Standard industrial analog input voltage ranges are converted to the ADC input voltage range using high-voltage, zero-drift input amplifiers. All input ports are robustly protected up to ±36V reverse polarity and ±2kV surge pulses without the need of TVS diodes.

Eight general-purpose digital I/O (GPIO) ports are available for common use, or they can be used to control external switches for configurable inputs.

The MAX22005 is factory calibrated with best-in-class system performance of less than 0.05% FSR Total-Unadjusted-Error (TUE) over temperature.

The host communicates with the MAX22005 through a high-speed 30MHz SPI bus for all configurations and information management, as well as for acquiring conversion results. An optional 8-bit CRC enhances the reliability of the SPI interface, protecting against all 8-bit bursts, as well as all double-bit errors.

The MAX22005 operates from 2.7V to 3.6V analog and digital supplies, and up to ±24V high-voltage supplies.

The MAX22005 is available in 48-pin LGA package and operates over the -40°C to +125°C industrial temperature range.

Applications

- Programmable Logic Controllers (PLC)
- Programmable Automation Controllers (PAC)
- Distributed Control Systems (DCS)

Benefits and Features

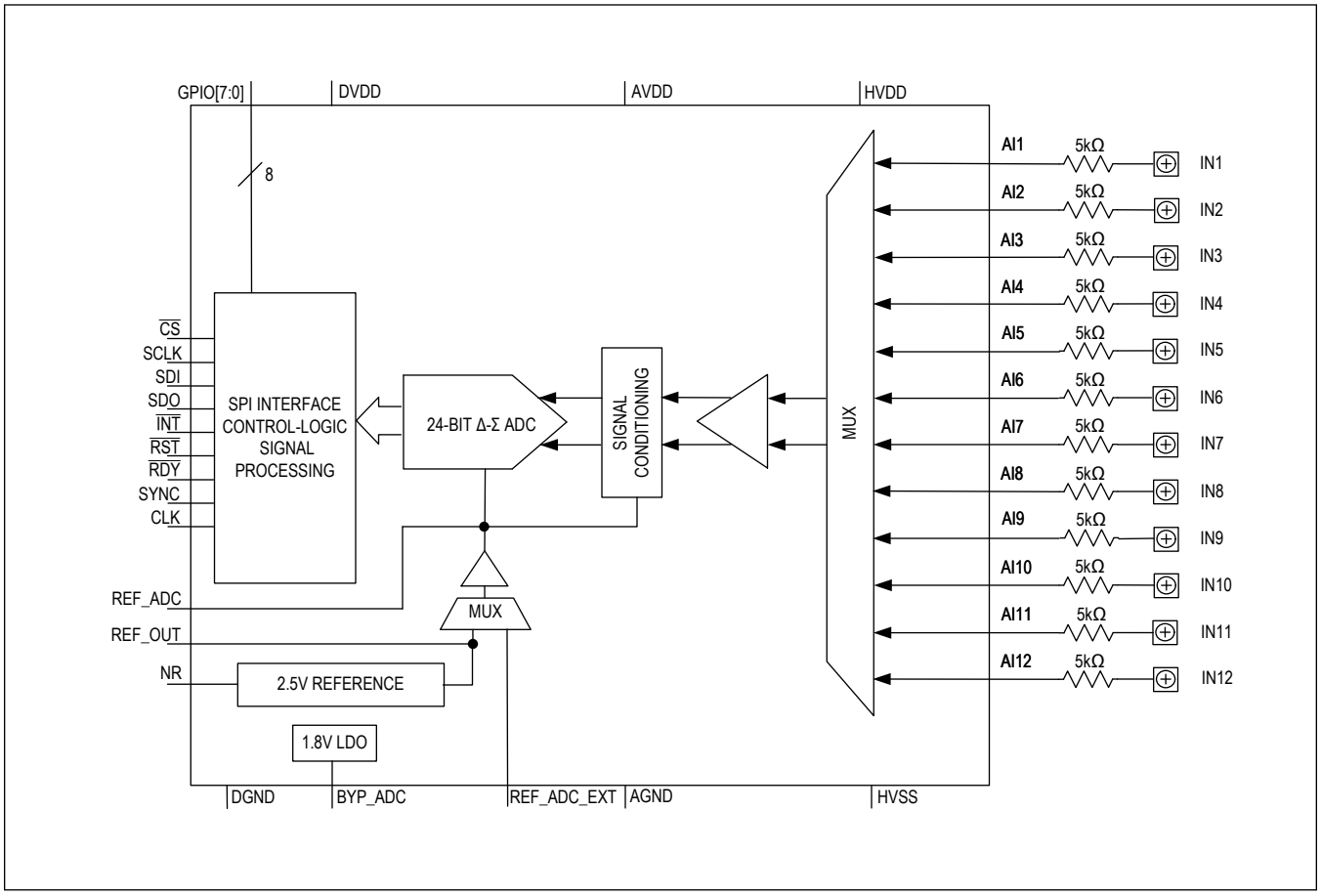
- Enables More Robust and Reliable Systems
  - ±36V High-Voltage Protection for All Input Ports
  - 2kV HBM ESD Protection of All Pins
  - ±2kV Surge Protection (with External 5kΩ Resistor)
  - CRC Detection for Robust Serial Communication
  - Watchdog Timer
- Software Configurability
  - ±12.5V Analog Input-Voltage Mode
  - ±25mA Analog Input-Current Mode Using External Sense Resistor
  - Configurable Inputs Using External Sense Resistor and Low-Cost Switches
- Best-in-Class System Accuracy
  - 0.02% FSR at 25°C Factory Calibrated
  - 0.05% FSR over ±50°C from 25°C Factory Calibration
  - Maximum of 30nA Input Leakage
  - 5ppm/°C Internal Reference
- Additional Features
  - Internal or External ADC Reference
  - Eight GPIO Ports
  - 48.5mW Low Power Dissipation with ±5V Supply
  - 30MHz SPI/QSPI/DSP-Compatible Serial Interface
- Operating Temperature -40°C to +125°C
- 7.5mm × 7mm 48-pin LGA package

***Ordering Information* appear at end of datasheet.**

19-101026; Rev 0; 4/21

maxim integrated™

Simplified Block Diagram



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Absolute Maximum Ratings

AVDD to AGND ..... -0.3V to +3.9V
DVDD to DGND ..... -0.3V to +3.9V
AGND to DGND ..... -0.3V to +0.3V
BYP_ADC to DGND ..... -0.3V to +2.1V
HVDD to HVSS ..... -0.3V to +52V
HVDD to AGND ..... -0.3V to +40V
AGND to HVSS ..... -0.3V to +40V
CS, SCLK, SDI, SDO, RDY, RST, SYNC, CLK, GPIO[7:0] to DGND ..... -0.3V to the lower of (+3.9V or V_{DVDD} + 0.3V)
REF_ADC, REF_ADC_EXT, NR, REF_OUT to AGND ..... -0.3V to the lower of (+3.9V or VAVDD + 0.3V)
AI_ to HVSS ..... -0.3V to the lower of (+52V or (V_{HVDD} - V_{HVSS}) + 0.3V)
INT to DGND ..... -0.3V to +6V
Maximum Current into Any Pin ..... ±50mA
Continuous Power Dissipation 48-pin LGA (JEDEC 2S2P PCB) (T_A = +70°C, derate 19.51mW/°C above +70°C.) 1560.98mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

48-PIN LGA

Package Code	L487A7M+1
Outline Number	21-100448
Land Pattern Number	90-100160
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	51.25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	23.46°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = -15V, Reference Source = Internal Reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25ºC.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT-VOLTAGE MODE—SINGLE-ENDED						
Headroom		From V_{HVSS}	2.5			V
		From V_{HVDD}	2.5			
Input-Voltage Range	V_{IN}	ADC full-scale range		±12.5		V
		Linear range V_{HVSS} = -5V, V_{HVDD} = +5V (*Note 2*)	-2.5		+2.5	
		Linear range (*Note 2*)	-10.5		+10.5	
Offset Error	V_{OFFSET}	T_A = +25°C		±0.1	±1.3	mV
Offset Drift		T_A = +25°C ± 50°C, with internal reference (*Note 3*)			±13.6	µV/°C
Gain Error		T_A = +25°C		±200	±450	ppm

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = -15V, Reference Source = Internal Reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25ºC.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Drift		T_A = +25°C ± 50°C, with internal reference (*Note 3*)			±3.4	ppm/°C
INL Error	INL	T_A = +25°C			±600	µV
INL Drift		T_A = +25°C ± 50°C (*Note 3*)			±4.0	µV/°C
Total Unadjusted Error	TUE	T_A = +25°C (*Note 4*)			±0.02	% FSR
		T_A = +25°C ± 50°C (*Note 3* and *Note 4*)			±0.05	
Input-Voltage Noise	V_{NOISE}	ADC sample rate is 11.52ksps, ADC mode is Continuous Single-Cycle.		138		$µV_{RMS}$
Input Current					±30	nA
Supply-Rejection Ratio	PSRR	DC, V_{HVDD} = +5V to +24V		100		dB
		DC, V_{HVSS} = -24V to -5V		100		
Open Detector Resistance		From AI_ to V_{HVDD}		2		MΩ
		From AI_ to AGND		2		
50Hz/60Hz Normal-Mode Rejection		DCHNL_RATE[3:0] = 0b0010, 0b0011, 0b0100, 0b0101	87			dB
		DCHNL_RATE[3:0] = 0b0000, 0b0001	75			
Settling Time		V_{IN} changes from 0V to -10.5V or 0V to +10.5V, digital output reaches 1% of final value. ADC sample rate is 57.6ksps, ADC mode is Continuous.			0.2	ms
ANALOG INPUT VOLTAGE MODE—DIFFERENTIAL						
Input-Voltage Range	V_{IN}	ADC full-scale range		±25		V
		linear range (*Note 2*)	-21		+21	
Offset Error	V_{OFFSET}	T_A = +25°C		±0.2	±2.6	mV
Offset Drift		T_A = +25°C ± 50°C, with internal reference (*Note 3*)			±23.1	µV/°C
Gain Error		T_A = +25°C		±200	±450	ppm
Gain Drift		T_A = +25°C ± 50°C, with internal reference (*Note 3*)			±4.8	ppm/°C
INL Error	INL	T_A = +25°C			±1.2	mV
INL Drift		T_A = +25°C ± 50°C (*Note 3*)			±5.0	µV/°C
Total Unadjusted Error	TUE	T_A = +25°C (*Note 4*)			±0.02	% FSR
		T_A = +25°C ± 50°C (*Note 3* and *Note 4*)			±0.05	
Input-Voltage Noise	V_{NOISE}	ADC sample rate is 11.52ksps, ADC mode is Continuous Single-Cycle.		275		$µV_{RMS}$
Common-Mode Rejection Ratio	CMRR	V_{CM} = -10V to +10V. Differential input is 0V	72			dB
Supply-Rejection Ratio	PSRR	DC, V_{HVDD} = +5V to +24V		100		dB
		DC, V_{HVSS} = -24V to -5V		100		
Input Current	I_{IN}				±30	nA

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = -15V, Reference Source = Internal Reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25ºC.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
50Hz/60Hz Normal-Mode Rejection		DCHNL_RATE[3:0] = 0b0010, 0b0011, 0b0100, 0b0101	87			dB
		DCHNL_RATE[3:0] = 0b0000, 0b0001	75			
Open-Detector Resistance		From AI_ to V_{HVDD}		2		MΩ
		From AI_ to AGND		2		
Settling Time		V_{IN} changes from 0V to -10.5V or 0V to +10.5V, digital output reaches 1% of final value. ADC sample rate is 57.6ksps; ADC mode is Continuous.			0.2	ms
ADC REFERENCE (REF_ADC)						
REF_ADC Output Voltage	V_{REF_ADC}	Internal reference		2.5		V
Output-Voltage Accuracy		Referred to V_{REF_ADC}, T_A = +25°C	-0.2		+0.2	%
Output-Voltage Temperature Coefficient		T_A = -40°C to +125°C (*Note 3*)		1	5	ppm/°C
Line Regulation		2.7V ≤ V_{AVDD} ≤ 3.6V			130	µV/V
REF_ADC Bypass Capacitor				4.7		µF
$V_{REF\_ADC\_EXT}$ Input Range		External Reference		2.5		V
DIGITAL INPUTS						
Input Logic-Low Voltage	V_{IL}				0.3 × V_{DVDD}	V
Input Logic-High Voltage	V_{IH}		0.7 × V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}		-1		+1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS						
Output Logic-Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Output Logic-High Voltage (SDO, RDYB, GPIO[7:0])	V_{OH}	I_{OH} = 4mA	0.9 × V_{DVDD}			V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				10		pF
SUPPLIES						
Analog Supply Voltage	V_{AVDD}		2.7	3.3	3.6	V
Digital Supply Voltage	V_{DVDD}		2.7	3.3	3.6	V

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = +15V, V_{HVSS} = -15V, Reference Source = Internal Reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25ºC.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive High-Voltage Supply	V_{HVDD}		5		24	V
Negative High-Voltage Supply	V_{HVSS}		-24		-5	V
High-Voltage Supply	V_{HV}	V_{HVDD} - V_{HVSS}	10		48	V
DVDD POR Threshold	V_{DVDD_POR}	Voltage rising		1.5		V
HVDD-HVSS Undervoltage Threshold		Voltage rising		1.5		V
Analog Supply Current	I_{AVDD}	ADC sample rate is 11.52ksps, ADC mode is Continuous Single-Cycle. Single-ended AI1–AI12 at AGND		4.5		mA
Digital Supply Current	I_{DVDD}	ADC sample rate is 11.52ksps, ADC mode is Continuous Single-Cycle. Single-ended AI1–AI12 at AGND		1.8		mA
High-Voltage Supply Current	I_{HV}	ADC sample rate is 11.52ksps, ADC mode is Continuous Single-Cycle. Single-ended AI1–AI12 at AGND		2.5		mA
Total Power		ADC sample rate is 11.52ksps, ADC mode is Continuous Single-Cycle. Single-ended AI1–AI12 at AGND		95.8		mW
		AI1–AI12 at AGND, V_{HVDD} = 5V and V_{HVSS} = -5V, all inputs are on		45.8		
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}	All SPI transactions			30	MHz
SCLK Clock Period	t_{CP}	All SPI transactions	33			ns
SCLK Pulse-Width High	t_{CH}	All SPI transactions	13			ns
SCLK Pulse-Width Low	t_{CL}	All SPI transactions	13			ns
$\overline{CS}$ Fall Setup Time	t_{CSS0}	$\overline{CS}$ falling edge to 1st SCLK rising edge setup time	7			ns
$\overline{CS}$ Fall Hold Time	t_{CSH0}	SCLK rising edge to $\overline{CS}$ falling edge hold time	0			ns
$\overline{CS}$ Rise Hold Time	t_{CSH1}	SCLK falling edge to $\overline{CS}$ rising edge hold time	3			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}	Minimum $\overline{CS}$ pulse-width high	150			ns
SDI Setup Time	t_{DS}	SDI setup time to SCLK rising edge	5			ns
SDI Hold Time	t_{DH}	SDI hold time after SCLK rising edge	5			ns
SDO Transition Time	t_{DOT}	SDO transition valid after SCLK falling edge			20	ns
SDO Hold Time	t_{DOH}	Output remains valid after falling edge of SCLK	2			ns
SDO Disable Time	t_{DOD}	$\overline{CS}$ rising edge to SDO disable, C_{LOAD} = 20pF			25	ns

Note 1: Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.

Note 2: Offset error, gain error, INL error, TUE, and settling times are only guaranteed in the linear range. The minimum and maximum specification of the linear range are guaranteed through offset, gain, INL error, and TUE.

Note 3: Guaranteed by design and characterization. Not tested in production.

Note 4: FSR stands for full-scale range. It is 25V in single-ended mode and 50V in differential mode.

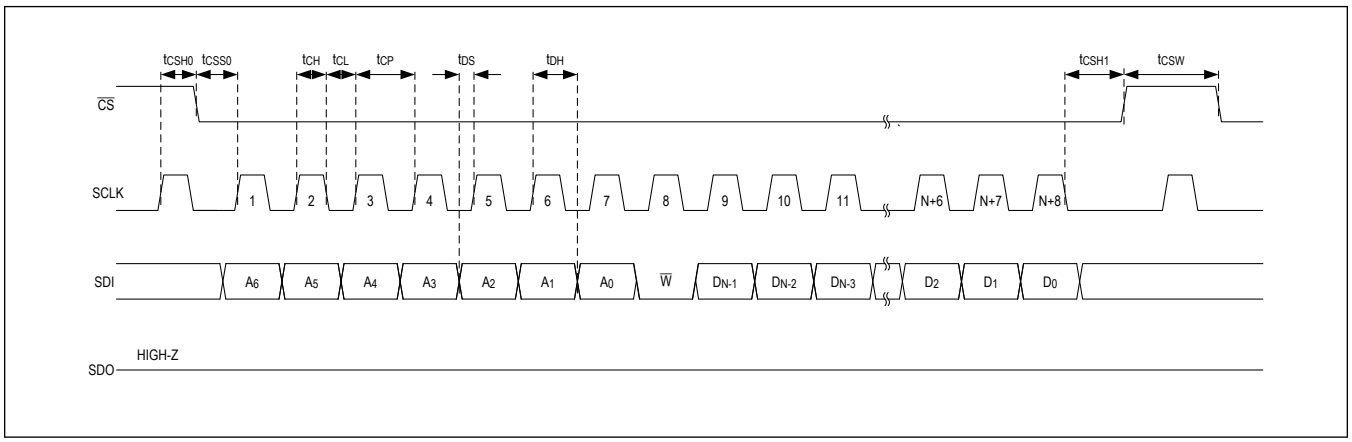


Figure 1. SPI Write Timing (N = 24 when CRC is Disabled and N = 32 when CRC is Enabled)

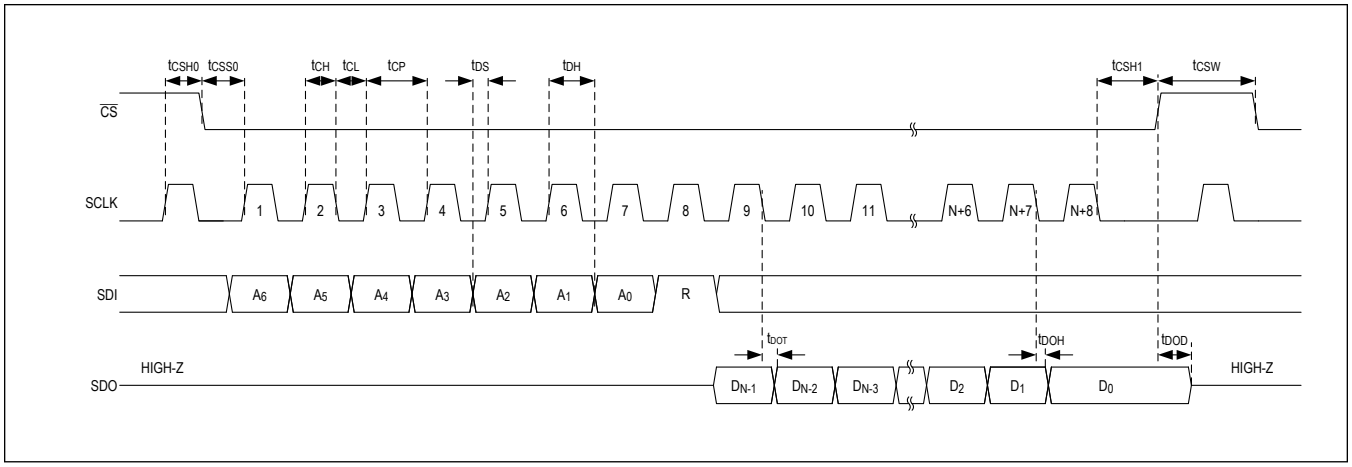
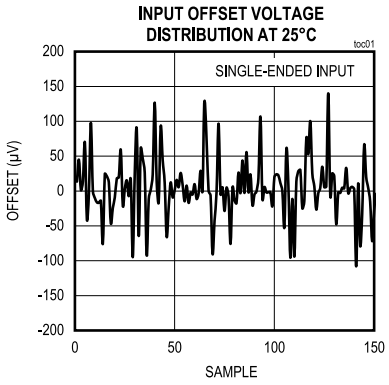
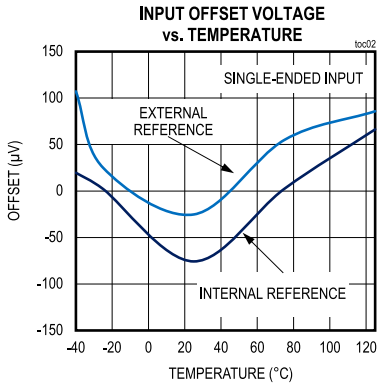


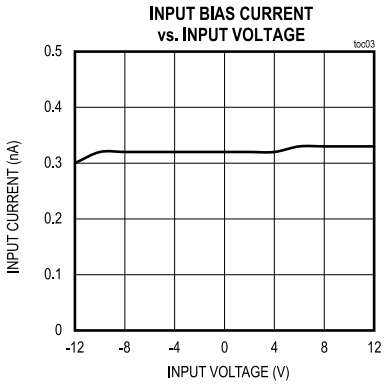
Figure 2. SPI Read Timing (N = 24 when CRC is Disabled and N = 32 when CRC is Enabled)

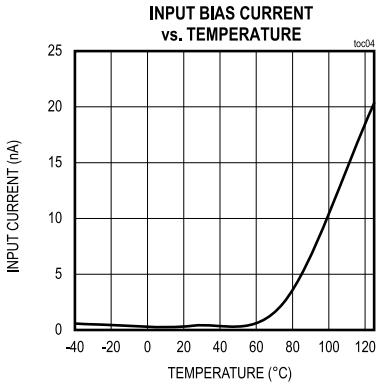
Typical Operating Characteristics

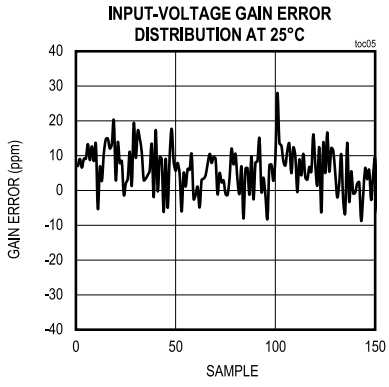
(V_{AVDD} = V_{DVDD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = -15V, T_A = +25°C, unless otherwise noted.)

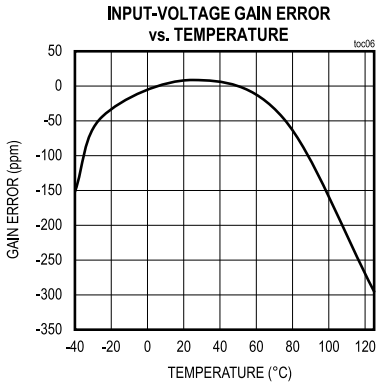


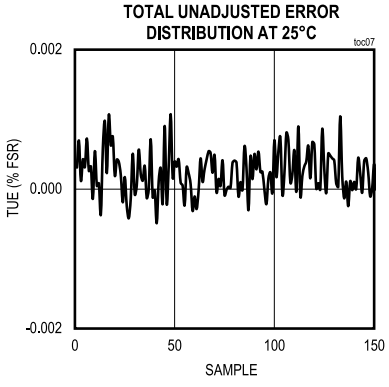


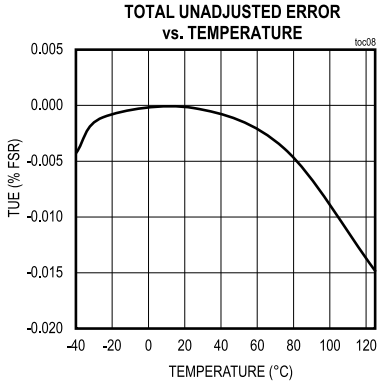


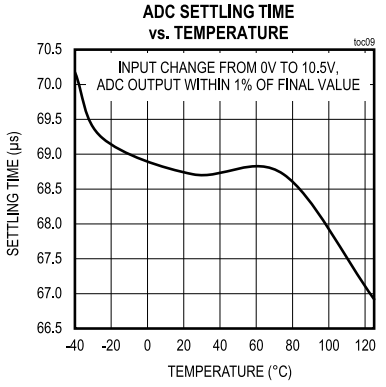






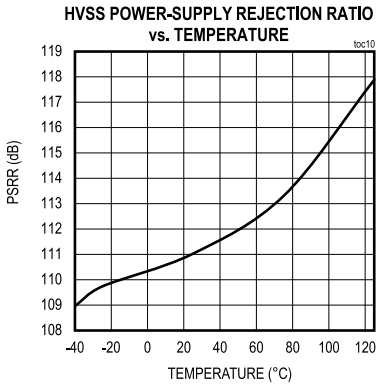


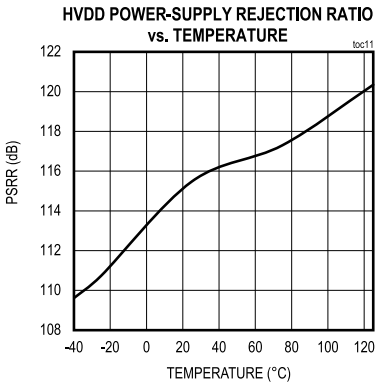




Typical Operating Characteristics (continued)

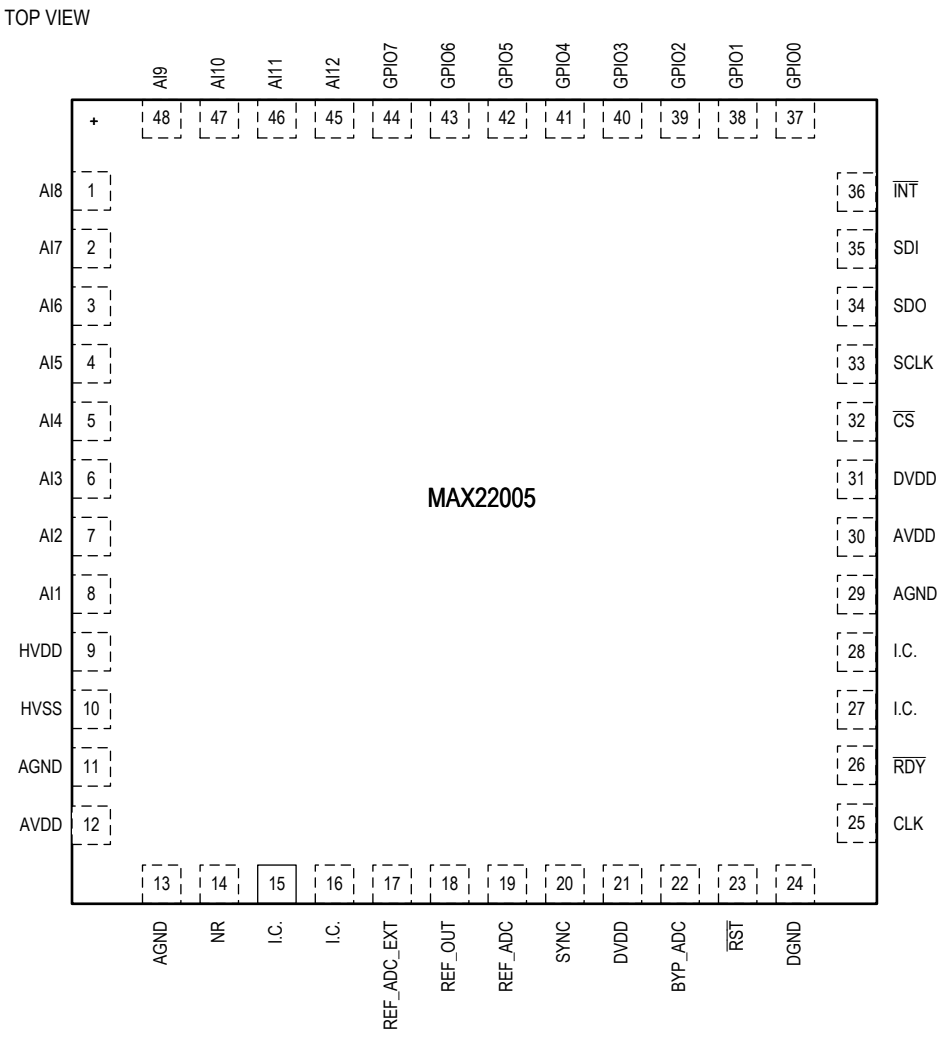
(V_{AVDD} = V_{DVDD} = +3.3V, V_{HVDD} = +15V, V_{HVSS} = -15V, T_A = +25°C, unless otherwise noted.)





Pin Configuration

MAX22005



LGA
7.5mm x 7.0mm

Pin Description

PIN	NAME	FUNCTION
ANALOG INPUTS		
1	AI8	Analog Input 8
2	AI7	Analog Input 7
3	AI6	Analog Input 6

Pin Description (continued)

PIN	NAME	FUNCTION
4	AI5	Analog Input 5
5	AI4	Analog Input 4
6	AI3	Analog Input 3
7	AI2	Analog Input 2
8	AI1	Analog Input 1
45	AI12	Analog Input 12
46	AI11	Analog Input 11
47	AI10	Analog Input 10
48	AI9	Analog Input 9
POWER		
9	HVDD	Positive High-Voltage Power Supply for the Input Path, +5V to +24V. Bypass HVDD to AGND through a 1µF capacitor.
10	HVSS	Negative High-Voltage Power Supply for the Input Path, -5V to -24V. Bypass HVSS to AGND through a 1µF capacitor.
11, 13, 29	AGND	Analog Ground. Connect all AGND pins together.
12, 30	AVDD	Analog Power Supply, 2.7V to 3.6V. Connect all AVDD together. Bypass each AVDD through a 1µF ceramic capacitor to AGND.
21, 31	DVDD	Digital Power Supply, 2.7V to 3.6V. Connect all DVDD together. Bypass each DVDD pin through a 1µF ceramic capacitor to DGND.
24	DGND	Digital Ground
REFERENCE AND INTERFACE		
14	NR	Voltage Reference Noise Reduction. Bypass NR through a 1µF ceramic capacitor to AGND to improve wideband noise.
15, 16, 27, 28	I.C.	Internally Connected. Connect to AGND for proper use.
17	REF_ADC_EXT	ADC External Voltage-Reference Input. Connect to AGND if not used.
18	REF_OUT	Voltage Reference Output. Bypass REF_OUT through a (0.1µF || 1µF) ceramic capacitor to AGND.
19	REF_ADC	ADC Voltage Reference-Buffered Output. Bypass REF_ADC through a 4.7µF ceramic capacitor to AGND.
20	SYNC	ADC Synchronization Input. SYNC resets the ADC modulator and digital filters. Connect SYNC of multiple MAX22005s in parallel to synchronize their ADCs to an external trigger and external clock. Connect SYNC to DGND if not used.
22	BYP_ADC	1.8V Sub-Regulator Output. Bypass BYP_ADC through a 220nF or larger capacitor to DGND.
23	$\overline{RST}$	Active-Low Reset Input. Keep $\overline{RST}$ high for normal operation.
25	CLK	External Clock Input. Connect to DGND if not used.
26	$\overline{RDY}$	Active-Low Data Ready Output. $\overline{RDY}$ goes low when a new ADC conversion result is available in the data register. When a read operation of a full output word completes, $\overline{RDY}$ returns high. $\overline{RDY}$ is always driven.
32	$\overline{CS}$	Active-Low SPI Chip-Select Input
33	SCLK	SPI Serial Clock Input
34	SDO	SPI Serial Data Output
35	SDI	SPI Serial Data Input
36	$\overline{INT}$	Interrupt Output. $\overline{INT}$ is an open-drain active-low output.

Pin Description (continued)

PIN	NAME	FUNCTION
GPIO PORTS		
37	GPIO0	General Purpose I/O 0
38	GPIO1	General Purpose I/O 1
39	GPIO2	General Purpose I/O 2
40	GPIO3	General Purpose I/O 3
41	GPIO4	General Purpose I/O 4
42	GPIO5	General Purpose I/O 5
43	GPIO6	General Purpose I/O 6
44	GPIO7	General Purpose I/O 7

Detailed Description

The MAX22005 is an industrial-grade configurable analog-input solution. The MAX22005 offers twelve single-ended inputs, six pairs of adjacent differential inputs, or eight multifunctional differential pairs defined around four triplets of inputs. A triplet of inputs is shown in Figure 3. The port INA would be the “common” input, while INC and the middle port, INB, would be the other two ports defining the triplet of inputs.

The pairing of ports are illustrated in Figure 4. The inputs highlighted in yellow are the common inputs (COM).

The MAX22005 provides a high-performance 24-bit delta-sigma ADC in the receive path. A high-performance decimation filter following the ADC provides a minimum of 87dB rejection for 50Hz/60Hz at select ADC data rates. The device includes a high-performance 5ppm/°C (max) voltage reference on-chip. However, external references can optionally be used.

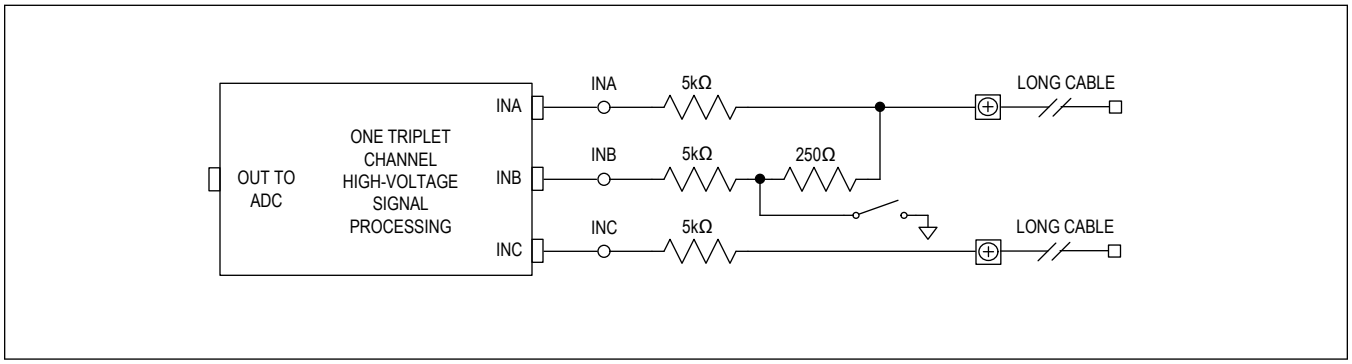


Figure 3. Input Port Triplet

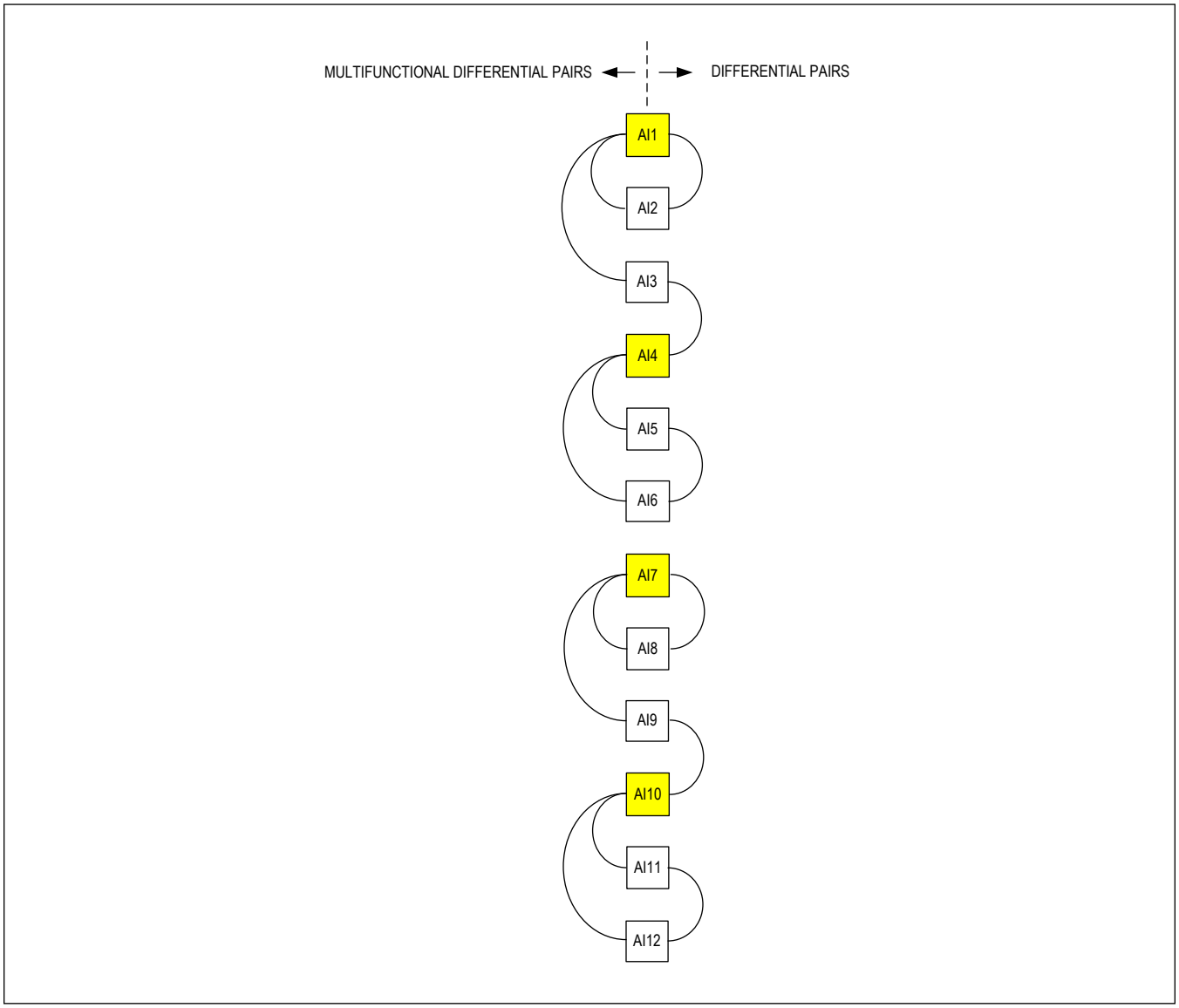


Figure 4. Input Ports Pairs

Modes of Operation

The MAX22005 offers the following modes of operation:

- 12 single-ended analog inputs
- 6 differential analog inputs
- 8 multifunctional differential analog inputs

Switching among those modes does not require changing the printed circuit board (PCB). The inputs can be configured for analog input-voltage mode (AIVM) or analog input-current mode (AICM). Current measurements by the MAX22005 rely on an external precision resistor to convert the current to voltage. For current measurements, one can use any odd channel input and its sense port. The integrated GPIO port can control an external analog switch to connect or disconnect the current-sense resistor electronically (refer to Figure 3). The external switches do not need to be accurate since the

current measurement is performed differentially. We recommend 2.5Ω low voltage CMOS switches.

The MAX22005 supports two-wire configuration for all single-ended and differential inputs, and three-wire configuration for multifunctional differential inputs, which could be used, for example, for a resistance temperature detector (RTD) connection. Refer to *AN7413* for other possible configuration options.

Input Range Settings

To maintain best accuracy, the MAX22005 provides multiple voltage ranges for its inputs.

Table 1 summarizes available ranges. The nominal range specifies the range for the intended application. The linear range encompasses the nominal range, where performance specifications such as gain error, offset error, INL, PSRR, and CMRR are still guaranteed. Even wider, the full-scale range sets the conversion limits of the data converter. This extended range defines the input-voltage limits that can be converted without clipping the ADC.

The MAX22005 sets the linear range at 105% of the nominal range, and the full-scale range at 125% of the nominal range. For example, for a ±10V nominal range, the MAX22005 provides a linear range of ±10.5V and a full-scale range of ±12.5V.

Table 1. Input Ranges

MODE	SETTING	NOMINAL	LINEAR	FULL SCALE
AIVM	±12.5V	±10V	±10.5V	±12.5V
AICM	±25mA	±20mA	±21mA	±25mA

Differential-Input Common-Mode Range

If the signal amplitude is less than the full-scale range of an input, the MAX22005 permits a greater input common-mode range.

The maximum allowed input common-mode range is calculated as follows:

$V_{CM} = 25 - V_{DIFF}$

where,

V_{CM} = Maximum input common-mode range

V_{DIFF} = Peak-to-peak input voltage

Input-Voltage Rating

All high-voltage analog inputs are ±36V tolerant with respect to AGND. In general, the following scenario at an analog input is depicted in Figure 5. Every analog input must have a series 5kΩ protection resistor. As long as the supply voltages at HVSS and HVDD are actively driven, the voltage at the MAX22005 input pin does not swing more than one diode voltage drop above HVDD or below HVSS. Since the series resistor limits the current, the diode voltage drop is small.

If one of the DC-DC converter malfunctions and is no longer capable of sinking or sourcing current, then the resistive feedback network around the DC-DC converter can be used to effectively protect the input pin of the MAX22005. It is the engineer's responsibility to design the total resistance R_{PATH} of the current path such that the voltages at the analog input pins of MAX22005 do not exceed their voltage ratings.

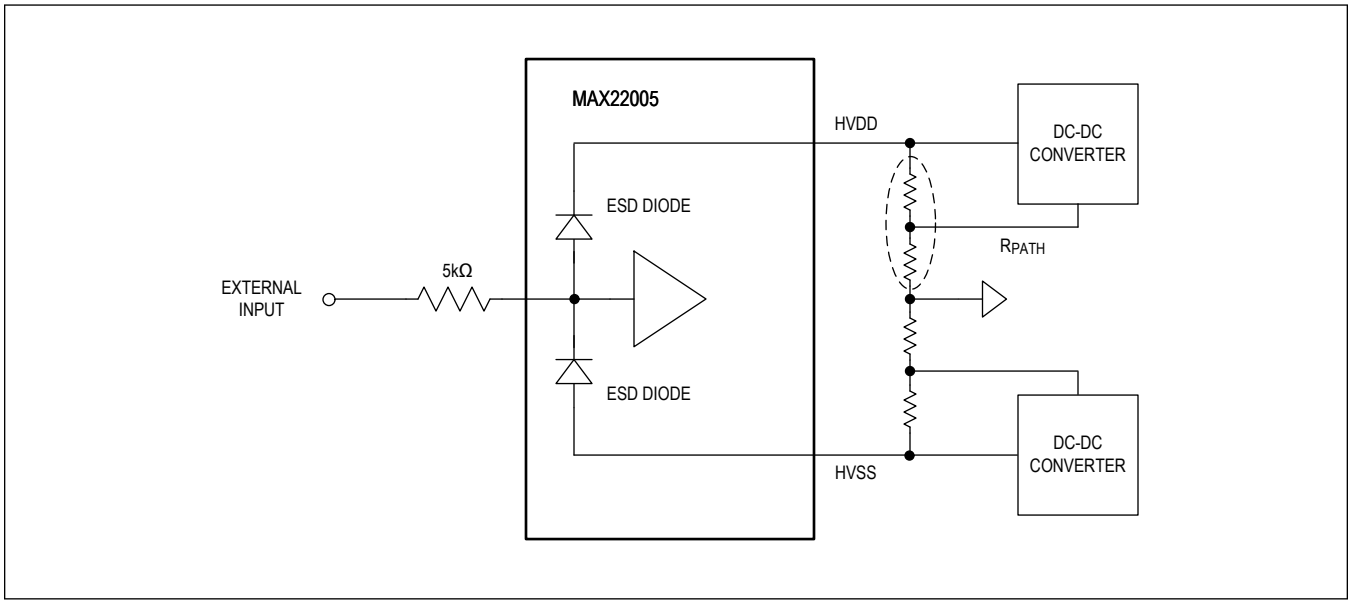


Figure 5. Input Protection

Supply Voltages and Power-Supply Sequencing

The MAX22005 has three independent supplies: a low-voltage analog supply (AVDD, AGND), a low-voltage digital supply (DVDD, DGND), both specified at 2.7V to 3.6V, and an analog bipolar high-voltage supply (HVDD, HVSS for the input AFE). For the high-voltage AFE to operate properly, the V_{HVSS} supply needs to be less than or below -5V and the V_{HVDD} supply needs to be greater than or equal to 5V. For ±12V inputs, at least V_{HVSS} = -15V and V_{HVDD} = 15V are required. The three supplies pairs (AVDD/AGND, DVDD/DGND, HVDD/HVSS) can be powered up in any order.

Power-On Reset

The AVDD and DVDD supplies are monitored by power-on reset circuitry. The MAX22005 is held in a reset state until the AVDD and DVDD supplies have reached a certain threshold that allows safe operations without loss of data. Once this threshold is exceeded, the SPI interface and low-voltage circuitry are fully functional. The high-voltage supply is also constantly monitored. The MAX22005 needs only the AVDD and DVDD supplies to communicate over the SPI interface. With AVDD and DVDD powered, loss of the high-voltage supply is reported through the HVDD_INT bit in the GEN_INT register.

SPI Interface

An SPI interface allows communication of all important information between a microprocessor and the MAX22005. An optional CRC enhances confidence in the data communicated to and from the MAX22005. This feature, disabled by default after a hardware reset or power-up (but not a software reset), can be enabled or disabled at any time through the SPI interface.

The SPI transactions are 40-bits long if CRC is enabled as shown in Table 2. If CRC is disabled, the SPI transactions are 32-bits long, as shown in Table 3.

Table 2. SPI Transaction with CRC Enabled

BITS 39:33	BIT 32	BITS 31:8	BITS 7:0
Register Address	R/$\overline{W}$	24-bit Payload	CRC

Table 3. SPI Transaction with CRC Disabled

BITS 31:25	BIT 24	BITS 23:0
Register Address	R/$\overline{W}$	24-bit Payload

The MAX22005 implements the CRC-8/MAXIM algorithm with an 0x31 polynomial ($x^8 + x^5 + x^4 + x^0$), the same polynomial that is used in Maxim's 1-wire® products. This CRC algorithm uses reflected input and output bytes (i.e., LSB first instead of MSB first on a byte basis; the byte order of the input sequence is not changed). The initial value is 0x00, and the output is reported as is without any XOR operation.

This CRC can detect the following types of errors:

- Any odd number of errors anywhere within the 32-bit number
- All double-bit errors anywhere within the 32-bit number
- Any cluster of errors that can be contained within an 8-bit window (1–8 bits incorrect)
- Most large clusters of errors

For write transactions, the CRC is calculated on the 32 bits that precede it, namely the 7-bit register address, 1-bit read or write control, and the 24-bit payload.

Here are two examples of write operations:

Write 0x00_0F00 to register GEN_CHNL_CTRL: 0x06_000F_0011

Write 0x34_0000 to register CHNL_CMD: 0x40_3400_00A0

For read transactions, the CRC sent by the MAX22005 back to the host is calculated on 32 bits made of the 8-bit header received from the host (register address and read control) and the 24 bits of payload.

Here are two examples of read operations:

Read the default value from register GEN_CNFG: 0x05_1000_00CB

Read the default value from register DCHNL_STA: 0x43_0000_08AA

CRC is disabled by default. Refer to *AN27* for more details.

Watchdog Timer

The MAX22005 features a watchdog timer for additional security of losing communication with the host controller. The watchdog can be enabled in the GEN_CNFG register (0x02) by setting the TMOUT_EN bit and setting up the TMOUT_CNFG, and TMOUT_SEL[3:0] bits for a desired interrupt behavior and timeout duration. The interrupt is asserted on the $\overline{INT}$ pin and in TMOUT_INT bit in the GEN_INT register (0x07) if the duration between two properly formatted SPI transactions exceeds the timeout period. A properly formatted transaction is a transaction that has a minimum of 32 bits (if CRC is disabled) or 40 bits (if CRC is enabled). A properly formatted transaction is always accounted for at the end of the transaction. Refer to the Register Map descriptions for more information.

Product Tracking

The MAX22005 includes a 32-bit wide unique serial number used for device tracking (SERIAL[32:0] in registers GEN_PROD and GEN_REV).

In addition, an eight-bit product ID that helps to distinguish different parts of the industrial I/O family (PROD_ID[7:0] in register GEN_PROD). The product ID can be decoded as follows:

Table 4. Product ID

BIT 7	6	5	4	3	2	1	0
Number of output Channels			Number of Input Channels				RTD/TC Support

The MAX22005 can accept up to 12 input channels; the product ID is 0x18.

The revision of the silicon is reflected in the eight-bit revision ID (REV_ID[7:0] in register GEN_REV).

Analog Input ADC

The analog input channels share one high-performance 24-bit delta-sigma analog-to-digital converter (ADC). The data

rate is programmable from 1sps (samples per second) to 115.2ksps. The ADC can utilize either the internal 2.5V reference or an external reference. The ADC services a total of 26 input configurations, which are selectable through bits AI_DCHNL_SEL[4:0] in register GEN_CHNL_CTRL. Table 5 summarizes the channel selection options.

Table 5. Input-Channel Configuration Selection

AI_DCHNL_SEL[4:0]	INPUT CONFIGURATION
00000	Input AI1 in single-ended mode (-12.5V to +12.5V range)
00001	Input AI2 in single-ended mode (-12.5V to +12.5V range)
00010	Input AI3 in single-ended mode (-12.5V to +12.5V range)
00011	Input AI4 in single-ended mode (-12.5V to +12.5V range)
00100	Input AI5 in single-ended mode (-12.5V to +12.5V range)
00101	Input AI6 in single-ended mode (-12.5V to +12.5V range)
00110	Input AI7 in single-ended mode (-12.5V to +12.5V range)
00111	Input AI8 in single-ended mode (-12.5V to +12.5V range)
01000	Input AI9 in single-ended mode (-12.5V to +12.5V range)
01001	Input AI10 in single-ended mode (-12.5V to +12.5V range)
01010	Input AI11 in single-ended mode (-12.5V to +12.5V range)
01011	Input AI12 in single-ended mode (-12.5V to +12.5V range)
01100	Inputs AI1–AI2 in differential mode (-25.0V to +25.0V range)
01101	Inputs AI3–AI4 in differential mode (-25.0V to +25.0V range)
01110	Inputs AI5–AI6 in differential mode (-25.0V to +25.0V range)
01111	Inputs AI7–AI8 in differential mode (-25.0V to +25.0V range)
10000	Inputs AI9–AI10 in differential mode (-25.0V to +25.0V range)
10001	Inputs AI11–AI12 in differential mode (-25.0V to +25.0V range)
10010	Inputs AI1(COM)–AI2 in multifunctional differential mode (-25.0V to +25.0V range)
10011	Inputs AI1(COM)–AI3 in multifunctional differential mode (-25.0V to +25.0V range)
10100	Inputs AI4(COM)–AI5 in multifunctional differential mode (-25.0V to +25.0V range)
10101	Inputs AI4(COM)–AI6 in multifunctional differential mode (-25.0V to +25.0V range)
10110	Inputs AI7(COM)–AI8 in multifunctional differential mode (-25.0V to +25.0V range)
10111	Inputs AI7(COM)–AI9 in multifunctional differential mode (-25.0V to +25.0V range)
11000	Inputs AI10(COM)–AI11 in multifunctional differential mode (-25.0V to +25.0V range)
11001	Inputs AI10(COM)–AI12 in multifunctional differential mode (-25.0V to +25.0V range)

The ADC results are stored in register DCHNL_DATA in two's complement format. Table 6 summarizes the ADC output codes and corresponding input voltages.

Table 6. Input-Channel Limit Values and Codes

AI_DCHNL_SEL[4:0]	INPUT CHANNEL	ADC CODE 0x800000 (-8388608) (V)	ADC CODE 0x000000 (0) (V)	ADC CODE 0x7FFFFF (+8388607) (V)
00000	AI1 single-ended	-12.5	0	+12.5
00001	AI2 single-ended	-12.5	0	+12.5
00010	AI3 single-ended	-12.5	0	+12.5
00011	AI4 single-ended	-12.5	0	+12.5
00100	AI5 single-ended	-12.5	0	+12.5
00101	AI6 single-ended	-12.5	0	+12.5
00110	AI7 single-ended	-12.5	0	+12.5

Table 6. Input-Channel Limit Values and Codes (continued)

AI_DCHNL_SEL[4:0]	INPUT CHANNEL	ADC CODE 0x800000 (-8388608) (V)	ADC CODE 0x000000 (0) (V)	ADC CODE 0x7FFFFF (+8388607) (V)
00111	AI8 single-ended	-12.5	0	+12.5
01000	AI9 single-ended	-12.5	0	+12.5
01001	AI10 single-ended	-12.5	0	+12.5
01010	AI11 single-ended	-12.5	0	+12.5
01011	AI12 single-ended	-12.5	0	+12.5
01100	AI1–AI2 differential	-25.0	0	+25.0
01101	AI3–AI4 differential	-25.0	0	+25.0
01110	AI5–AI6 differential	-25.0	0	+25.0
01111	AI7–AI8 differential	-25.0	0	+25.0
10000	AI9–AI10 differential	-25.0	0	+25.0
10001	AI11–AI12 differential	-25.0	0	+25.0
10010	AI1(COM)–AI2 multifunctional differential	-25.0	0	+25.0
10011	AI1(COM)–AI3 multifunctional differential	-25.0	0	+25.0
10100	AI4(COM)–AI5 multifunctional differential	-25.0	0	+25.0
10101	AI4(COM)–AI6 multifunctional differential	-25.0	0	+25.0
10110	AI7(COM)–AI8 multifunctional differential	-25.0	0	+25.0
10111	AI7(COM)–AI9 multifunctional differential	-25.0	0	+25.0
11000	AI10(COM)–AI11 multifunctional differential	-25.0	0	+25.0
11001	AI10(COM)–AI12 multifunctional differential	-25.0	0	+25.0

The mode of operation is selected using the DCHNL_MODE[1:0] bits in register DCHNL_CMD. By default, the ADC is in standby mode to reduce the overall power consumption.

The delta-sigma modulator is followed by a chain of high-performance digital filters, consisting of a fifth-order SINC filter, an averaging filter, and a fourth-order SINC filter, depending on the data rate chosen. Several data rates offer at least 75dB of 50Hz or 60Hz suppression.

The ADC offers three conversion modes of operation: continuous mode, single-cycle mode, and continuous single-cycle mode.

In **continuous mode**, the ADC operates continuously at the selected sample rate. Based on the data rate, the digital filter requires up to five output samples to settle. This mode is used when data from a single channel is collected, and a high sample rate is desired.

Single-cycle mode offers a single-cycle no-latency conversion, after which the ADC goes back into standby mode. This mode is used when single measurements on several channels are made, and a moderate sample rate is required.

In **continuous single-cycle mode** the ADC performs continuous no-latency conversions at the selected rate. This mode is used if continuous monitoring of one channel is required, but settling of the digital filters should be masked. This is useful in the case if a quick settling after a change in the input is desired, but the increased data rate in continuous mode is not required.

The modes of operation are selected using bits SCYCLE and CONTSC in register DCHNL_CTRL1. Continuous mode and continuous single-cycle mode can be exited by changing the DCHNL_MODE[1:0] bits in register DCHNL_CMD to standby mode. In addition, any change to the input channel selection (bits AI_DCHNL_SEL[4:0] in register GEN_CHNL_CTRL), the ADC control registers (DCHNL_CTRL1, DCHNL_CTRL2) also abort any ongoing continuous conversion and return the ADC to standby mode.

The available data rates are selected by setting bits DCHNL_RATE[3:0] in register DCHNL_CMD. Table 7 summarizes the data rates that are available in continuous mode. The data rates in bold offer 50Hz and/or 60Hz suppression in excess

of 75dB. Note that system calibration correction cannot be selected for the highest data rate.

Table 7. Selection of Data Rates for Continuous Conversion

DCHNL_RATE[3:0]	DATA RATE (SPS)	EFFECTIVE NUMBER OF BITS
0000	**5**	21
0001	**10**	21
0010	**15**	21
0011	**30**	20
0100	**50**	20
0101	**60**	20
0110	225	19
0111	450	19
1000	900	19
1001	1800	18
1010	3600	18
1011	7200	18
1100	14400	17
1101	28800	17
1110	57600	17
1111	115200 (Note)	16

Note: System calibration is not supported with the highest data rate.

Table 8 shows the data rates available in single-cycle mode. Operation in single-cycle mode requires an overhead at the beginning of a conversion to allow the analog front-end of the ADC to settle. In addition, time is required to process the raw modulator output. The nominal data rate is shown in Table 8, as it is an indication of the sampling period of the input signal. The actual data rate depends on whether system calibration is used or not, as the computational overhead is different in the two cases. The data rates in bold offer 50Hz and/or 60Hz suppression in excess of 75dB.

Table 8. Selection of Data Rates for Single-Cycle Conversion

DCHNL_RATE[3:0]	NOMINAL DATA RATE (sps)	ACTUAL DATA RATE (sps)	ACTUAL DATA RATE PLUS SYSTEM CALIBRATION (sps)	EFFECTIVE NUMBER OF BITS
0000	**1 (0.9955)**	**1 (0.9955)**	**1 (0.9955)**	21
0001	**2.5**	**2.5**	**2.5**	21
0010	**5**	**5**	**5**	21
0011	**10**	**10**	**10**	20
0100	**12.5**	**12.5**	**12.5**	20
0101	**15**	**15**	**15**	20
0110	50	50	50	19
0111	60	60	60	19
1000	150	150	150	19
1001	300	299	298	18
1010	900	891	886	18
1011	1800	1772	1752	18
1100	2880	2810	2759	17
1101	5760	5486	5297	17
1110	11520	10473	9804	17
1111	23040	19200	17067	16

Table 9 shows the data rates available in single-cycle continuous mode. The single-cycle continuous mode operation is similar to single-cycle mode, but the overhead is slightly different, and therefore the actual data rates differ slightly as well. Again, the data rates in bold offer 50Hz and/or 60Hz suppression in excess of 75dB.

Table 9. Selection of Data Rates for Single-Cycle Continuous Conversion

DCHNL_RATE[3:0]	NOMINAL DATA RATE (sps)	ACTUAL DATA RATE (sps)	ACTUAL DATA RATE PLUS SYSTEM CALIBRATION (sps)	EFFECTIVE NUMBER OF BITS
0000	**1 (0.9955)**	**1 (0.9955)**	**1 (0.9955)**	21
0001	**2.5**	**2.5**	**2.5**	21
0010	**5**	**5**	**5**	21
0011	**10**	**10**	**10**	20
0100	**12.5**	**12.5**	**12.5**	20
0101	**15**	**15**	**15**	20
0110	50	50	50	19
0111	60	60	60	19
1000	150	150	150	19
1001	300	299	299	18
1010	900	892	887	18
1011	1800	1776	1755	18
1100	2880	2818	2768	17
1101	5760	5519	5327	17
1110	11520	10593	9910	17
1111	23040	19609	17389	16

The ADC offers a status bit to signal an overrange condition. If the output of the digital filter overflows, bit DOR in register DCHNL_STA is set to logic high. In this case, the digital output is set to 0x7FFFFF if a positive overflow occurs, or to 0x800000 if a negative overflow occurs.

Analog Input Offset and Gain Error Calibration

System Calibration

The MAX22005 is factory calibrated to satisfy its TUE specification. However, the user is able to perform their own system-level calibration to eliminate gain and offset errors of the entire analog input signal chain, including board level components. A two-point measurement algorithm can be used to calculate and correct the system level offset and gain error. Separate pairs of offset and gain correction registers are provided in the MAX22005 for each of the 26 input configurations. The two-point calibration to calculate both gain and offset coefficients is depicted in Figure 6. Refer to *AN7449* "MAX22005 User Calibration Guide" for more information.

Before attempting a user/system calibration, the offset and gain calibration registers (DCHNL_N_SOC and DCHNL_N_SGC) of the respective channel should be set to 0x00_0000 and 0xC0_0000, respectively.

Two input voltages V_1 and V_2 that are close to the application full-scale range must be applied, and the corresponding digital output codes C_1 and C_2, respectively, are recorded.

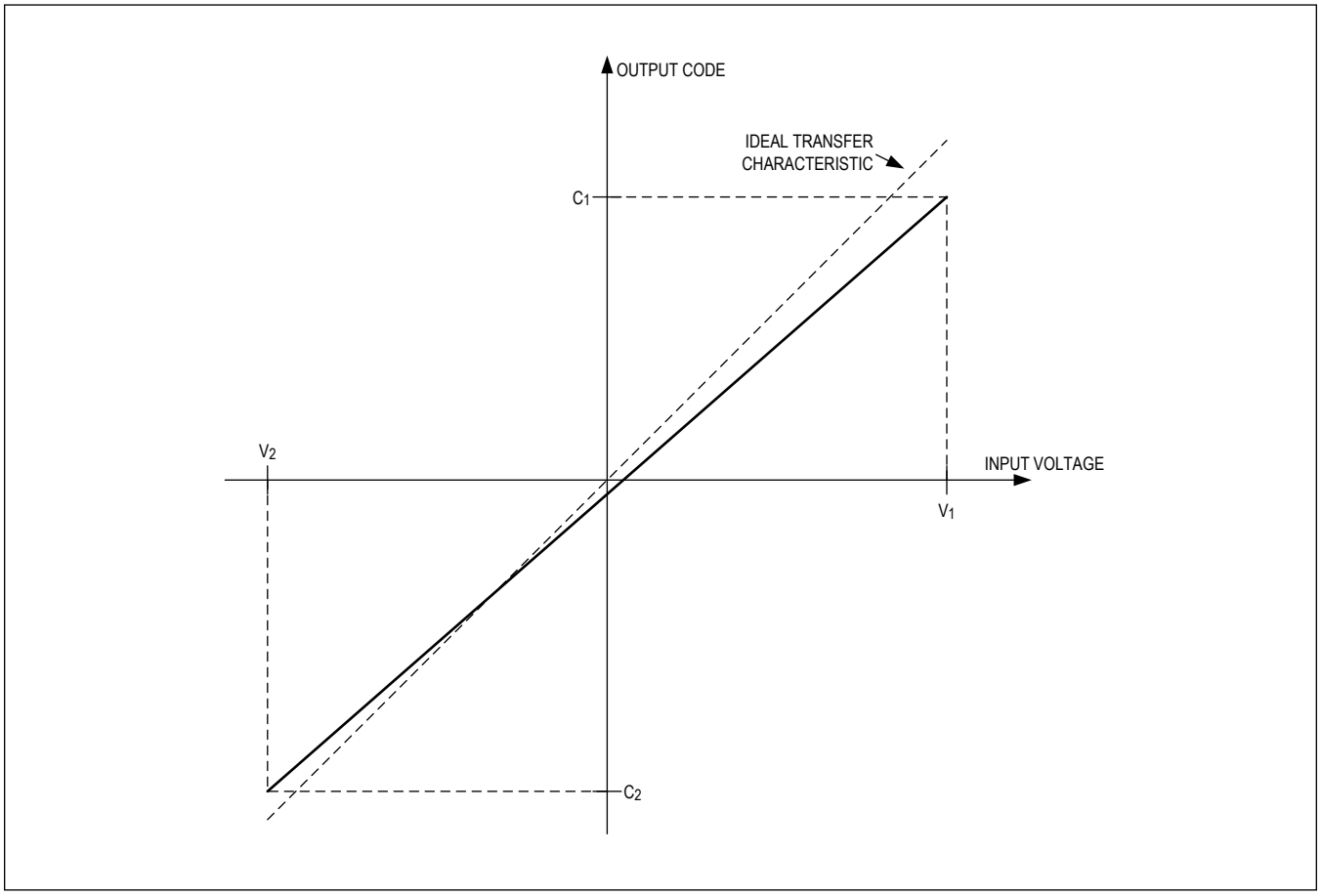


Figure 6. Two Point System Calibration

The gain A of the input channel can then be calculated as follows:

$$A = \frac{(\frac{C_1 - C_2}{2^{24}}) \times V_{FSR}}{(V_1 - V_2)}$$

where V_{FSR} is the full-scale range of the input channel selected. The full-scale range for each channel is shown in Table 10.

Table 10. Full-Scale Range of Input Channels

AI_DCHNL_SEL[4:0]	INPUT CHANNEL	FULL_SCALE RANGE V_{FSR} (V)	DIGITAL GAIN A_{DIG}	DIGITAL SIGN S_{DIG}
00000	AI1 single-ended	25	2	+1
00001	AI2 single-ended	25	2	-1
00010	AI3 single-ended	25	2	-1
00011	AI4 single-ended	25	2	+1
00100	AI5 single-ended	25	2	+1
00101	AI6 single-ended	25	2	-1

Table 10. Full-Scale Range of Input Channels (continued)

00110	AI7 single-ended	25	2	+1
00111	AI8 single-ended	25	2	-1
01000	AI9 single-ended	25	2	-1
01001	AI10 single-ended	25	2	+1
01010	AI11 single-ended	25	2	+1
01011	AI12 single-ended	25	2	-1
01100	AI1–AI2 differential	50	2	+1
01101	AI3–AI4 differential	50	2	-1
01110	AI5–AI6 differential	50	2	+1
01111	AI7–AI8 differential	50	2	+1
10000	AI9–AI10 differential	50	2	-1
10001	AI11–AI12 differential	50	2	+1
10010	AI1(COM)–AI2 multifunctional differential	50	2	+1
10011	AI1(COM)–AI3 multifunctional differential	50	2	+1
10100	AI4(COM)–AI5 multifunctional differential	50	2	+1
10101	AI4(COM)–AI6 multifunctional differential	50	2	+1
10110	AI7(COM)–AI8 multifunctional differential	50	2	+1
10111	AI7(COM)–AI9 multifunctional differential	50	2	+1
11000	AI10(COM)–AI11 multifunctional differential	50	2	+1
11001	AI10(COM)–AI12 multifunctional differential	50	2	+1

The gain calibration coefficient can now be calculated by dividing the default gain calibration coefficient by the calculated gain:

gain calibration coefficient = 1.5/A.

The result is expressed in unsigned binary format with a fraction length of 23 bits and loaded into the appropriate DCHNL_N_SGC register.

The input-referred offset can be calculated as

$$V_{OFFSET} = \frac{C_1 \times V_{FSR}}{2^{24}} - A \times V_1$$

In order to calculate the offset calibration coefficient, the digital gain A_{DIG} and the sign S_{DIG} of the signal chain needs to be taken into account. Both gain and sign are summarized in Table 9. With this information the offset calibration coefficient DCHNL_N_SOC can be calculated as follows:

$$DCHNL\_N\_SOC = \left(C_1 - A \times \frac{V_1}{V_{FSR}} \times 2^{24}\right) \times \frac{S_{DIG}}{1.5 \times A_{DIG}}$$

The resulting value of DCHNL_N_SOC must be expressed in two's complement format.

The calculated calibration coefficients are stored in registers DCHNL_N_SOC for the offset calibration coefficient, and DCHNL_N_SGC for the gain calibration coefficient, respectively. These registers are selectable using indirect addressing (see the DCHNL_N_SEL register).

By default, the raw ADC output data is corrected using the system gain and offset calibration coefficients. However, the correction can be disabled using bits NOSYSG and NOSYSO bits in register DCHNL_CTRL2.

ADC Software Reset

The host can issue a software reset to restore the default state of the ADC. A software reset sets the DCHNL_ registers back into their default states and resets the internal state machines. However, a software reset does not execute the complete power-on reset or hardware reset sequence. A software reset is, thus, not effective if e.g., the SPI interface does not respond.

Two SPI transactions are required to issue a software reset: first, bit DCHNL_PD in register DCHNL_CTRL1 must be set to logic high (reset). Then a write transaction to register DCHNL_CMD must be issued with DCHNL_MODE[1:0] set to '01'.

To confirm the completion of the reset operation, bits PDSTAT[1:0] in register DCHNL_STA must be monitored. While the ADC is in its reset phase, PDSTAT[1:0] is set to '11' (reset). After the reset operation is complete, PDSTAT[1:0] is set to '10' (standby). It is usually not required to monitor the reset ('11') state. Polling for standby mode ('10') is sufficient.

ADC $\overline{RDY}$ (Data Ready) Output

$\overline{RDY}$ indicates the ADC conversion status and the availability of the conversion result. When $\overline{RDY}$ is low, a conversion result is available. When $\overline{RDY}$ is high, a conversion is in progress, and the data for the current conversion is not available. $\overline{RDY}$ is driven high after a complete read of the DCHNL_DATA register. If the data is read after each sample becomes available, $\overline{RDY}$ transitions from high-to-low at the output data rate. If the previous data was not read, then $\overline{RDY}$ transitions from low-to-high approximately 0.5µs before new data becomes available. A falling edge on $\overline{RDY}$ then indicates the availability of new data. In continuous mode, $\overline{RDY}$ remains high for the first four conversion results and on the 5th result, $\overline{RDY}$ goes low to indicate valid data.

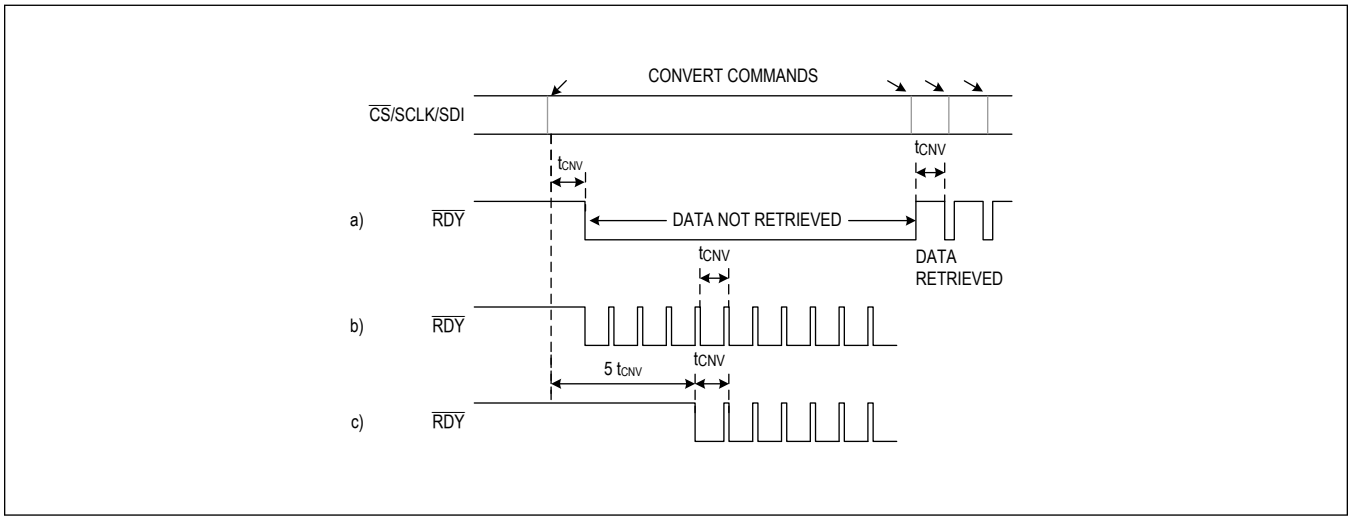


Figure 7. RDY Output Timing, a) Single-Cycle Mode, b) Continuous Single-Cycle Mode, c) Continuous Conversion Mode

ADC Conversion Synchronization Using the SYNC Pin

The MAX22005 incorporates a highly stable internal oscillator, providing a nominal system clock of 7.3728MHz (8.192MHz x 0.9) for both analog and digital timing. Optionally, a highly stable external clock can be used. The SYNC pin, ideally in conjunction with an external clock, can be used to synchronize the data conversions to external events. Although the synchronization method also works with an internal clock, resynchronization is inevitable due to local oscillators with limited frequency accuracy. A highly stable external clock that can be shared by multiple MAX22005s allows for much longer time intervals without the requirement of resynchronization.

Set bit SYNC_MODE in register DCHNL_CTRL2 to logic high to enable external synchronization mode. Also, SCYCLE in register DCHNL_CTRL1 must be set to logic zero, as SYNC_MODE is operational only for the continuous conversion mode. Optionally, set bit EXTCLK in register DCHNL_CTRL2 to logic high to use a highly accurate external clock signal.

The synchronization mode is used to detect if the current conversions are synchronized to a continuous-pulse signal with a period greater than the data rate. The pulse-width of the synchronization signal is not critical, as only the rising edge of the synchronization pulse is used as a timing reference. The pulse-width, however, must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. In addition, the low time of the SYNC signal between consecutive SYNC pulses must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. Ideally, the frequency of the synchronization signal is an integer multiple of the conversion rate. The synchronization mode records the number of ADC clock cycles between a falling edge of $\overline{RDY}$ and the rising edge of the next SYNC pulse. At the following SYNC pulse, the number of ADC clock cycles between a falling edge of $\overline{RDY}$ and the rising edge of the SYNC pulse is evaluated again and compared to the recorded value. If the new number of ADC clock cycles differs by more than one from the recorded value, the conversion in progress is stopped, the digital filter contents are reset, and a new conversion starts. As the digital filter is reset, the full digital filter latency is required before valid results are available. If the new ADC clock count is within the ±1 count limit, the conversions continue uninterrupted.

Figure 8 shows the timing relationship between the MAX22005 ADC clock and the SYNC signal. Due to startup delays, any SYNC pulses before the first falling edge of $\overline{RDY}$ are ignored. The first rising edge on the SYNC pin after a falling edge of $\overline{RDY}$ establishes the relationship between the SYNC signal and the conversion timing.

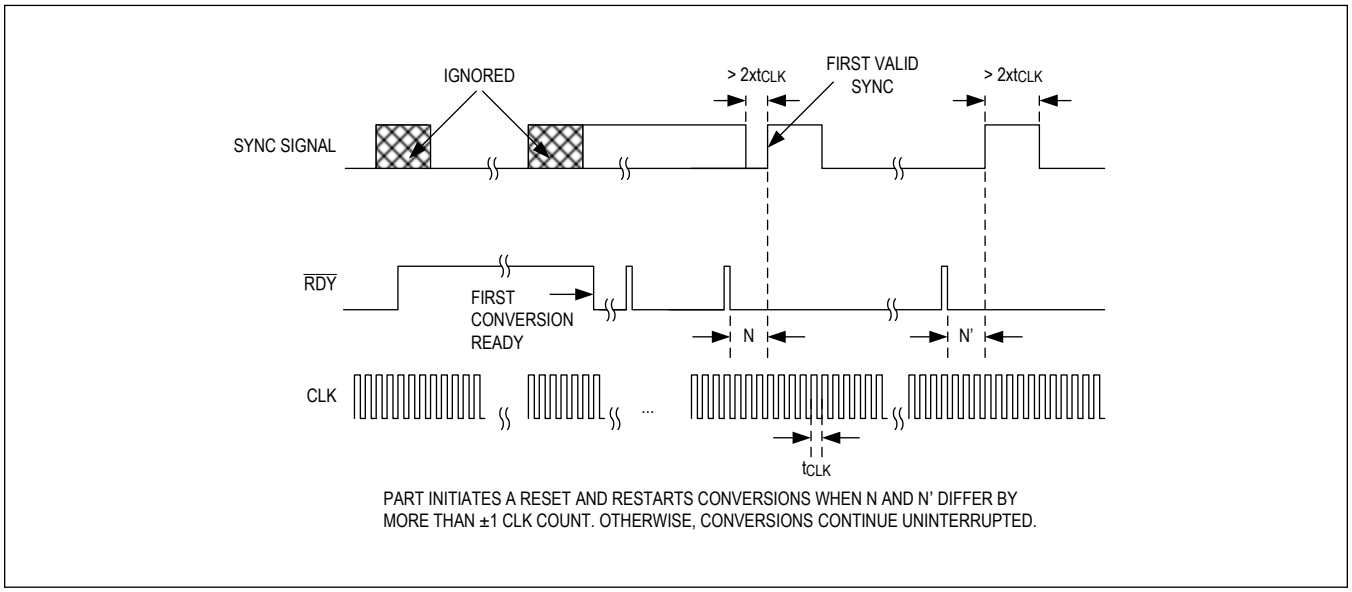


Figure 8. SYNC Input Timing

Hardware Reset

The MAX22005 features an active-low $\overline{RST}$ pin to perform a hardware reset. Pulling the $\overline{RST}$ pin low reconfigures all registers to the power-on reset state. All analog inputs are disconnected. Any ADC conversion in progress is stopped, and the digital filters are reset. When $\overline{RST}$ goes back to logic "1," the part behaves the same way as when power is first applied.

Register Map

MAX22005 Register Map

ADDRESS	NAME	MSB							LSB
GEN Registers									
0x00	GEN_PROD[23:16]	PROD_ID[7:0]							
	GEN_PROD[15:8]	SERIAL_MSB[15:8]							
	GEN_PROD[7:0]	SERIAL_MSB[7:0]							
0x01	GEN_REV[23:16]	REV_ID[7:0]							
	GEN_REV[15:8]	SERIAL_LSB[15:8]							
	GEN_REV[7:0]	SERIAL_LSB[7:0]							
0x02	GEN_CNFG[23:16]	CRC_EN	–	ADCREF_SEL	–	–	–	–	–
	GEN_CNFG[15:8]	–	–	–	–	–	–	–	–
	GEN_CNFG[7:0]	–	–	TMOUT_EN	TMOUT_CNFG	TMOUT_SEL[3:0]			
0x03	GEN_CHNL_CTRL[23:16]	AIP_TEST[1:0]		AIN_TEST[1:0]		–	–	–	–
	GEN_CHNL_CTRL[15:8]	–	–	–	AI_DCHNL_SEL[4:0]				
	GEN_CHNL_CTRL[7:0]	–	–	–	–	–	–	–	–
0x04	GEN_GPIO_CTRL[23:16]	GPIO_EN[7:0]							
	GEN_GPIO_CTRL[15:8]	GPIO_DIR[7:0]							
	GEN_GPIO_CTRL[7:0]	GPO_DATA[7:0]							
0x05	GEN_GPI_INT[23:16]	GPI_POS_EDGE_INT[7:0]							
	GEN_GPI_INT[15:8]	GPI_NEG_EDGE_INT[7:0]							
	GEN_GPI_INT[7:0]	–	–	–	–	–	–	–	–
0x06	GEN_GPI_DATA[23:16]	GPI_POS_EDGE_INT_STA[7:0]							
	GEN_GPI_DATA[15:8]	GPI_NEG_EDGE_INT_STA[7:0]							
	GEN_GPI_DATA[7:0]	GPI_DATA[7:0]							
0x07	GEN_INT[23:16]	–	–	–	–	–	–	–	–
	GEN_INT[15:8]	–	–	–	–	–	–	TMOUT_INT	–
	GEN_INT[7:0]	HVDD_INT	–	–	–	–	CNFG_INT	CRC_INT	GPI_INT
0x08	GEN_INTEN[23:16]	–	–	–	–	–	–	–	–
	GEN_INTEN[15:8]	–	–	–	–	–	–	TMOUT_INTEN	–
	GEN_INTEN[7:0]	HVDD_INTEN	–	–	–	–	CNFG_INTEN	CRC_INTEN	GPI_INTEN
0x09	GEN_PWR_CTRL[23:16]	–	–	–	–	GEN_PD	–	GEN_RST	–
	GEN_PWR_CTRL[15:8]	–	–	–	–	–	–	–	–
	GEN_PWR_CTRL[7:0]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
DCHNL Registers									
0x20	DCHNL_CMD[23:16]	–	–	DCHNL_MODE[1:0]		DCHNL_RATE[3:0]			
	DCHNL_CMD[15:8]	–	–	–	–	–	–	–	–
	DCHNL_CMD[7:0]	–	–	–	–	–	–	–	–
0x21	DCHNL_STA[23:16]	–	–	–	–	–	–	–	–
	DCHNL_STA[15:8]	–	REFDET	–	–	–	–	DOR	–
	DCHNL_STA[7:0]	RATE[3:0]				PDSTAT[1:0]		MSTAT	RDY
0x22	DCHNL_CTRL1[23:16]	–	–	–	DCHNL_PD	–	–	SCYCLE	CONTSC
	DCHNL_CTRL1[15:8]	–	–	–	–	–	–	–	–
	DCHNL_CTRL1[7:0]	–	–	–	–	–	–	–	–
0x23	DCHNL_CTRL2[23:16]	EXTCLK	–	SYNC_MODE	–	NOSYSG	NOSYSO	–	–
	DCHNL_CTRL2[15:8]	–	–	–	–	–	–	–	–
	DCHNL_CTRL2[7:0]	–	–	–	–	–	–	–	–
0x24	DCHNL_DATA[23:16]	DCHNL_DATA[23:16]							
	DCHNL_DATA[15:8]	DCHNL_DATA[15:8]							
	DCHNL_DATA[7:0]	DCHNL_DATA[7:0]							
0x25	DCHNL_N_SEL[23:16]	–	–	–	–	–	–	–	–
	DCHNL_N_SEL[15:8]	–	–	–	–	–	–	–	–
	DCHNL_N_SEL[7:0]	–	–	DCHNL_OTP_SEL	DCHNL_N_SEL[4:0]				
0x26	DCHNL_N_SOC[23:16]	DCHNL_N_SOC[23:16]							
	DCHNL_N_SOC[15:8]	DCHNL_N_SOC[15:8]							
	DCHNL_N_SOC[7:0]	DCHNL_N_SOC[7:0]							
0x27	DCHNL_N_SGC[23:16]	DCHNL_N_SGC[23:16]							
	DCHNL_N_SGC[15:8]	DCHNL_N_SGC[15:8]							
	DCHNL_N_SGC[7:0]	DCHNL_N_SGC[7:0]							

Register Details

GEN_PROD (0x0)

BIT	23	22	21	20	19	18	17	16
Field	PROD_ID[7:0]							
Reset	0x18							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	SERIAL_MSB[15:8]							
Reset	0xXX							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_MSB[7:0]							
Reset	0xXX							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROD_ID	23:16	8-bit product ID code
SERIAL_MSB	15:0	The most significant 16-bits of a 32-bit code unique to each MAX22005.

GEN_REV (0x1)

BIT	23	22	21	20	19	18	17	16
Field	REV_ID[7:0]							
Reset	0x00							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	SERIAL_LSB[15:8]							
Reset	0xXX							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	SERIAL_LSB[7:0]							
Reset	0xXX							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REV_ID	23:16	8-bit revision ID code
SERIAL_LSB	15:0	The least significant 16-bits of a 32-bit code unique to each MAX22005.

GEN_CNFG (0x2)

If an ADC conversion is in progress, every write to bit ADCREF_SEL aborts the ADC conversion unless the write transaction does not result in a change of the content of ADCREF_SEL.

BIT	23	22	21	20	19	18	17	16
Field	CRC_EN	–	ADCREF_SEL	–	–	–	–	–
Reset	0b0	–	0b0	–	–	–	–	–
Access Type	Write, Read	–	Write, Read	–	–	–	–	–
BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	TMOUT_EN	TMOUT_CNFG	TMOUT_SEL[3:0]			
Reset	–	–	0b0	0b0	0x0			
Access Type	–	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_EN	23	CRC checker enable	0b0: CRC checker disabled 0b1: CRC checker enabled
ADCREF_SEL	21	ADC voltage reference	0b0: Internal voltage reference 0b1: External voltage reference
TMOUT_EN	5	Timeout enable	0b0: Timeout disabled 0b1: Timeout enabled
TMOUT_CNFG	4	Timeout configuration	0b0: When the timeout period expires, TMOUT_INT is asserted. 0b1: When the timeout period expires, TMOUT_INT is asserted, and the register field GPIO_EN[7:0] is reset, which disables all GPIO ports.
TMOUT_SEL	3:0	Timeout duration selection	0x0: 100ms 0x1: 200ms 0x2: 300ms 0x3: 400ms 0x4: 500ms 0x5: 600ms 0x6: 700ms 0x7: 800ms 0x8: 900ms 0x9: 1.0s 0xA: 1.1s 0xB: 1.2s 0xC: 1.3s 0xD: 1.4s 0xE: 1.5s 0xF: 1.6s

GEN_CHNL_CTRL (0x3)

If an ADC conversion is in progress, every write to bits AI_DCHNL_SEL[4:0] aborts the ADC conversion unless the write transaction does not result in a change of the content of AI_DCHNL_SEL[4:0].

BIT	23	22	21	20	19	18	17	16
Field	AIP_TEST[1:0]		AIN_TEST[1:0]		–	–	–	–
Reset	0x0		0x0		–	–	–	–
Access Type	Write, Read		Write, Read		–	–	–	–

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	AI_DCHNL_SEL[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
AIP_TEST	23:22	Diagnostic switches for AI1, AI4, AI5, AI7, AI10, and AI11	0x0: Diagnostic disabled 0x1: 2MΩ resistor to AGND 0x2: 2MΩ resistor to HVDD 0x3: 2MΩ resistor to both HVDD and AGND
AIN_TEST	21:20	Diagnostic switches for AI2, AI3, AI6, AI8, AI9, and AI12	0x0: Diagnostic disabled 0x1: 2MΩ resistor to AGND 0x2: 2MΩ resistor to HVDD 0x3: 2MΩ resistor to both HVDD and AGND
AI_DCHNL_SEL	12:8	Analog-input configuration selection If the host attempts to write a reserve state to this field, a configuration interrupt is issued (CNFG_INT) and the register field remains unchanged; thus, reflecting the last valid configuration selection.	0x0: AI1 single-ended 0x1: AI2 single-ended 0x2: AI3 single-ended 0x3: AI4 single-ended 0x4: AI5 single-ended 0x5: AI6 single-ended 0x6: AI7 single-ended 0x7: AI8 single-ended 0x8: AI9 single-ended 0x9: AI10 single-ended 0xA: AI11 single-ended 0xB: AI12 single-ended 0xC: AI1–AI2 differential 0xD: AI3–AI4 differential 0xE: AI5–AI6 differential 0xF: AI7–AI8 differential 0x10: AI9–AI10 differential 0x11: AI11–AI12 differential 0x12: AI1(COM)–AI2 multifunctional differential 0x13: AI1(COM)–AI3 multifunctional differential 0x14: AI4(COM)–AI5 multifunctional differential 0x15: AI4(COM)–AI6 multifunctional differential 0x16: AI7(COM)–AI8 multifunctionall differential 0x17: AI7(COM)–AI9 multifunctional differential 0x18: AI10(COM)–AI11 multifunctional differential 0x19: AI10(COM)–AI12 multifunctional differential 0x1A: reserved 0x1B: reserved 0x1C: reserved 0x1D: reserved 0x1E: reserved 0x1F: reserved

GEN_GPIO_CTRL (0x4)

BIT	23	22	21	20	19	18	17	16
Field	GPIO_EN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	GPIO_DIR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	GPO_DATA[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_EN	23:16	GPIO ports enable control. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: The corresponding GPIO is disabled (default) 1: The corresponding GPIO is enabled
GPIO_DIR	15:8	GPIO ports direction control. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: The corresponding GPIO is configured as an input port (default) 1: The corresponding GPIO is configured as output port
GPO_DATA	7:0	Data bits sent to the GPO-configured ports. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: The corresponding GPO set as logic low (default) 1: The corresponding GPO set as logic high

GEN_GPI_INT (0x5)

BIT	23	22	21	20	19	18	17	16
Field	GPI_POS_EDGE_INT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	GPI_NEG_EDGE_INT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_POS_EDGE_INT	23:16	Positive-edge detection control for signals received on GPI-configured ports. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: Positive-edge detection disabled on the corresponding GPI port (default) 1: Positive-edge detection enabled on the corresponding GPI port
GPI_NEG_EDGE_INT	15:8	Negative-edge detection control for signals received on GPI-configured ports. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: Negative-edge detection disabled on corresponding GPI port (default) 1: Negative-edge detection enabled on corresponding GPI port

GEN_GPI_DATA (0x6)

BIT	23	22	21	20	19	18	17	16
Field	GPI_POS_EDGE_INT_STA[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BIT	15	14	13	12	11	10	9	8
Field	GPI_NEG_EDGE_INT_STA[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BIT	7	6	5	4	3	2	1	0
Field	GPI_DATA[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_POS_EDGE_INT_STA	23:16	Each bit indicates if its corresponding GPI-configured port has detected a positive edge. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: No positive edge was detected on the corresponding GPI port (default) 1: At least one positive edge was detected on the corresponding GPI port
GPI_NEG_EDGE_INT_STA	15:8	Each bit indicates if its corresponding GPI-configured port has detected a negative edge. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: No negative edge was detected on the corresponding GPI port (default) 1: At least one negative edge was detected on the corresponding GPI port
GPI_DATA	7:0	Each bit contains the logic level applied to its corresponding GPI-configured port. The MSB corresponds to GPIO7 and the LSB to GPIO0.	0: Logic-level low detected at the GPI-configured port 1: Logic-level high detected at the GPI-configured port

GEN_INT (0x7)

BIT	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	TMOUT_INT	–
Reset	–	–	–	–	–	–	0b0	–
Access Type	–	–	–	–	–	–	Read Clears All	–

BIT	7	6	5	4	3	2	1	0
Field	HVDD_INT	–	–	–	–	CNFG_INT	CRC_INT	GPI_INT
Reset	0b0	–	–	–	–	0b0	0b0	0b0
Access Type	Read Only	–	–	–	–	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
TMOUT_INT	9	Asserted when the timeout duration expires if the timeout function is enabled. Cleared when read.	0b0: Timeout duration not expired 0b1: Timeout duration expired
HVDD_INT	7	Asserted when the high-voltage supply HVDD/HVSS falls below a preset threshold, indicating that the functionality of the amplifiers is not guaranteed. Cleared when the high-voltage supply exceeds the threshold again.	0b0: HVDD supply is above the preset threshold 0b1: HVDD supply is below the preset threshold
CNFG_INT	2	Asserted when the host selects states 0x1A to 0x1F for AI_DCHNL_SEL or DCHNL_N_SEL. Cleared when read.	0b0: No configuration error detected 0b1: Configuration error detected
CRC_INT	1	Asserted when a CRC error is detected when the CRC mode is enabled. Cleared when read.	0b0: No CRC error detected 0b1: CRC error detected
GPI_INT	0	Asserted when at least one positive or negative edge was detected at the input of at least one GPI-configured port. Cleared when read.	0b0: No edge detected on any GPI-configured port 0b1: At least one edge detected on at least one GPI-configured port

GEN_INTEN (0x8)

BIT	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	TMOUT_INTEN	–
Reset	–	–	–	–	–	–	0b0	–
Access Type	–	–	–	–	–	–	Write, Read	–
BIT	7	6	5	4	3	2	1	0
Field	HVDD_INTEN	–	–	–	–	CNFG_INTEN	CRC_INTEN	GPI_INTEN
Reset	0b0	–	–	–	–	0b0	0b0	0b0
Access Type	Write, Read	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TMOUT_INTEN	9	TMOUT interrupt enable	0b0: The corresponding interrupt cannot assert $\overline{INT}$ 0b1: The corresponding interrupt can assert $\overline{INT}$

BITFIELD	BITS	DESCRIPTION	DECODE
HVDD_INTEN	7	HVDD interrupt enable	0b0: The corresponding interrupt cannot assert $\overline{INT}$ 0b1: The corresponding interrupt can assert $\overline{INT}$
CNFG_INTEN	2	CNFG interrupt enable	0b0: The corresponding interrupt cannot assert $\overline{INT}$ 0b1: The corresponding interrupt can assert $\overline{INT}$
CRC_INTEN	1	CRC interrupt enable	0b0: The corresponding interrupt cannot assert $\overline{INT}$ 0b1: The corresponding interrupt can assert $\overline{INT}$
GPI_INTEN	0	GPI interrupt enable	0b0: The corresponding interrupt cannot assert $\overline{INT}$ 0b1: The corresponding interrupt can assert $\overline{INT}$

GEN_PWR_CTRL (0x9)

BIT	23	22	21	20	19	18	17	16
Field	–	–	–	–	GEN_PD	–	GEN_RST	–
Reset	–	–	–	–	0b0	–	0b0	–
Access Type	–	–	–	–	Write, Read	–	Write, Read	–

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_PD	19	Power-down control for the register GEN_CHNL_CTRL that controls the analog path settings	0b0: Normal operation 0b1: Power-down: Setting GEN_PD to logic high has an effect equivalent to powering down all input paths. When GEN_PD is set to logic low, the channels recover the configuration they had before GEN_PD was set to logic high. Therefore, no register needs to be reprogrammed after exiting power-down mode. Additionally, register contents can be modified while in power-down mode if desired.
GEN_RST	17	Soft-reset control for the register GEN_CHNL_CTRL that controls the analog path settings.	0b0: Normal operation 0b1: Reset mode: Setting GEN_RST is equivalent to clearing GEN_CHNL_CTRL register. Also, any on-going conversion is aborted. If a conversion was aborted, it needs to be restarted using DCHNL_CMD register.

DCHNL_CMD (0x20)

If an ADC conversion is in progress, every write transaction to the DCHNL_CMD register is ignored unless the write transaction puts the ADC in a power-down mode.

BIT	23	22	21	20	19	18	17	16
Field	–	–	DCHNL_MODE[1:0]		DCHNL_RATE[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read		Write, Read			

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DCHNL_MODE	21:20	Analog Input ADC mode	0x0: Reserved 0x1: Power down performed based on the DCHNL_PD setting 0x2: Reserved 0x3: Conversion mode
DCHNL_RATE	19:16	ADC data rates.	

DCHNL_STA (0x21)

BIT	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	15	14	13	12	11	10	9	8
Field	–	REFDET	–	–	–	–	DOR	–
Reset	–	0b0	–	–	–	–	0b0	–
Access Type	–	Read Only	–	–	–	–	Read Only	–

BIT	7	6	5	4	3	2	1	0
Field	RATE[3:0]				PDSTAT[1:0]		MSTAT	RDY
Reset	0x0				0x2		0b0	0b0
Access Type	Read Only				Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REFDET	14	Reference voltage detection (internal or external reference). This bit does not inhibit normal operation and is intended for status only. The value of the REFDET bit is valid within 30µs after a conversion start command and is invalid when not in conversion.	0b0: No reference voltage detected (reference voltage < 0.35V) 0b1: Reference voltage detected (reference voltage > 0.35V)
DOR	9	Digital overrange	0b0: The conversion result is within the digital operating range of the ADC 0b1: The conversion result has exceeded the maximum or minimum value of the converter and the result has been set to the maximum or minimum value.
RATE	7:4	RATE[3:0] indicates the conversion rate that corresponds to the results in the DCHNL_DATA register or the rate that was used for the calibration coefficient calculation. The corresponding RATE[3:0] is only valid until the DCHNL_DATA register is read.	Refer to Table 7, Table 8 and Table 9.
PDSTAT	3:2	Power states of the analog input ADC	0x0: Conversion mode 0x1: Reserved 0x2: Standby 0x3: Reset
MSTAT	1	ADC Status. Due to internal timing, the status update of MSTAT might be delayed up to 2µs after start or completion of a conversion. This delay should be taken into account if MSTAT is polled immediately after a status change.	0b0: The delta-sigma modulator is not converting 0b1: Conversion is in progress
RDY	0	A new conversion is result ready. A complete read of the DCHNL_DATA register deasserts this bit.	0b0: No new conversion result available 0b1: A new conversion result available

DCHNL_CTRL1 (0x22)

If an ADC conversion is in progress, every write transaction to the DCHNL_CTRL1 register aborts the ADC conversion unless the write transaction does not result in a change of the content of the register.

BIT	23	22	21	20	19	18	17	16
Field	–	–	–	DCHNL_PD	–	–	SCYCLE	CONTSC
Reset	–	–	–	0b0	–	–	0b1	0b0
Access Type	–	–	–	Write, Read	–	–	Write, Read	Write, Read
BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DCHNL_PD	20	Analog input ADC power-down state	0b0: Standby 0b1: Reset
SCYCLE	17	Single-cycle conversion mode	0b0: Continuous conversion mode (latency due to digital filtering) 0b1: Single-Cycle mode where a no-latency conversion is followed by a power-down to standby mode
CONTSC	16	Continuous single-cycle mode	0b0: Single conversion 0b1: Continuous single-cycle conversions

DCHNL_CTRL2 (0x23)

If an ADC conversion is in progress, every write transaction to the DCHNL_CTRL2 register aborts the ADC conversion unless the write transaction does not result in a change of the content of the register.

BIT	23	22	21	20	19	18	17	16
Field	EXTCLK	–	SYNC_MODE	–	NOSYSG	NOSYSO	–	–
Reset	0b0	–	0b0	–	0b0	0b0	–	–
Access Type	Write, Read	–	Write, Read	–	Write, Read	Write, Read	–	–

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EXTCLK	23	External clock selection	0b0: Internal oscillator 0b1: External clock
SYNC_MODE	21	External synchronization mode	0b0: Disabled 0b1: Enabled
NOSYSG	19	No system calibration gain correction	0b0: System calibration gain coefficient SGC is used to compute the final output data 0b1: System calibration gain coefficient SGC is not used to compute the final output data
NOSYSO	18	No system calibration offset correction	0b0: System calibration offset coefficient SOC is used to compute the final output data 0b1: System calibration offset coefficient SOC is not used to compute the final output data

DCHNL_DATA (0x24)

BIT	23	22	21	20	19	18	17	16
Field	DCHNL_DATA[23:16]							
Reset	0x000000							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	DCHNL_DATA[15:8]							
Reset	0x000000							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	DCHNL_DATA[7:0]							
Reset	0x000000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DCHNL_DATA	23:0	Analog input configuration conversion result in two's complement

DCHNL_N_SEL (0x25)

BIT	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	DCHNL_OTP_SEL	DCHNL_N_SEL[4:0]				
Reset	–	–	0b0	0x00				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DCHNL_OTP_SEL	5	Calibration coefficient selection	0b0: The DCHNL_N_SOC and DCHNL_N_SGC registers for the channel selected by DCHNL_N_SEL[4:0] can be modified through SPI transactions. 0b1: The SOC and SGC registers for the channel selected by DCHNL_N_SEL[4:0] are loaded with the corresponding factory calibrated coefficients, overwriting the current content of the selected SOC and SGC registers.
DCHNL_N_SEL	4:0	The value written in this register corresponds to the input configuration as defined for AI_DCHNL_SEL[4:0]. Once this register is written with the desired input configuration, the DCHNL_N_SOC and DCHNL_N_SGC registers for the selected input configuration can be modified through SPI transactions. If the host attempts to write a reserve state to this field (0x1A to 0x1F), a configuration interrupt is issued (CNFG_INT) and DCHNL_N_SEL remains unchanged; thus, reflecting the last valid entry.	

DCHNL_N_SOC (0x26)

If an ADC conversion is in progress, every write transaction to the DCHNL_N_SOC register is ignored if DCHNL_N_SEL[4:0] corresponds to the channel currently selected for conversion, and the register retains its current value. Write transactions to the DCHNL_N_SOC register if DCHNL_N_SEL[4:0] does not correspond to the channel currently selected for conversion are allowed, and the register is updated with the new value.

BIT	23	22	21	20	19	18	17	16
Field	DCHNL_N_SOC[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	15	14	13	12	11	10	9	8
Field	DCHNL_N_SOC[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DCHNL_N_SOC[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DCHNL_N_SOC	23:0	System offset calibration value for the input configuration selected by DCHNL_N_SEL[4:0] in two's complement format.

DCHNL_N_SGC (0x27)

If an ADC conversion is in progress, every write transaction to the DCHNL_N_SGC register is ignored if

DCHNL_N_SEL[4:0] corresponds to the channel currently selected for conversion, and the register retains its current value. Write transactions to the DCHNL_N_SGC register if DCHNL_N_SEL[4:0] does not correspond to the channel currently selected for conversion are allowed, and the register is updated with the new value.

BIT	23	22	21	20	19	18	17	16
Field	DCHNL_N_SGC[23:16]							
Reset	0xC00000							
Access Type	Write, Read							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	DCHNL_N_SGC[15:8]							
Reset	0xC00000							
Access Type	Write, Read							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DCHNL_N_SGC[7:0]							
Reset	0xC00000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DCHNL_N_SGC	23:0	System gain calibration value for the input configuration selected by DCHNL_N_SEL[4:0] in unsigned binary format with a fraction length of 23 bits, i.e., only the MSB is an integer bit. Examples: 0x80_0000 Gain of 1.0 0xC0_0000 Gain of 1.5 0xA0_0000 Gain of 1.25 0x60_0000 Gain of 0.75 Once the OTP outputs are stable after the deassertion of the power-on reset or the external reset, the corresponding OTP bank content is loaded into each DCHNL_N_SGC register. The register content value is approximately 1.5 (0xC0_0000) to counter the inherent signal-chain gain of 0.67, which is required by the delta-sigma modulator.

Applications Information

Power Supply Headroom Requirements

Analog inputs power from HVDD and HVSS, and generally need 2.5V of headroom to meet all linearity specifications. To accept ±10V inputs, whose full-scale range is ±12.5V, supply the MAX22005 with at least ±15V on HVDD/HVSS.

Any external reference voltage on the REF_ADC_EXT pin must never exceed V_{AVDD}. A schottky diode connected between REF_ADC_EXT and AVDD can help satisfy this requirement.

Power Supply Sequencing

The four supplies, AVDD, DVDD, HVDD and HVSS can power up in any order. Add a 1µF bypass capacitor between each supply pin and respected return (AGND or DGND) pin. It is recommended to supply HVDD and HVSS simultaneously.

Board Layout

Use proper grounding techniques such as a multilayer board with a low-inductance ground plane.

- Keep DGND separate from AGND, connecting the two at one point.
- Use a ground plane shielding to improve noise immunity.
- Keep analog signal traces away from digital signal traces, especially clock traces.

For a detailed recommended layout, refer to the MAX22005 EV kit data sheet.

Surge Protection

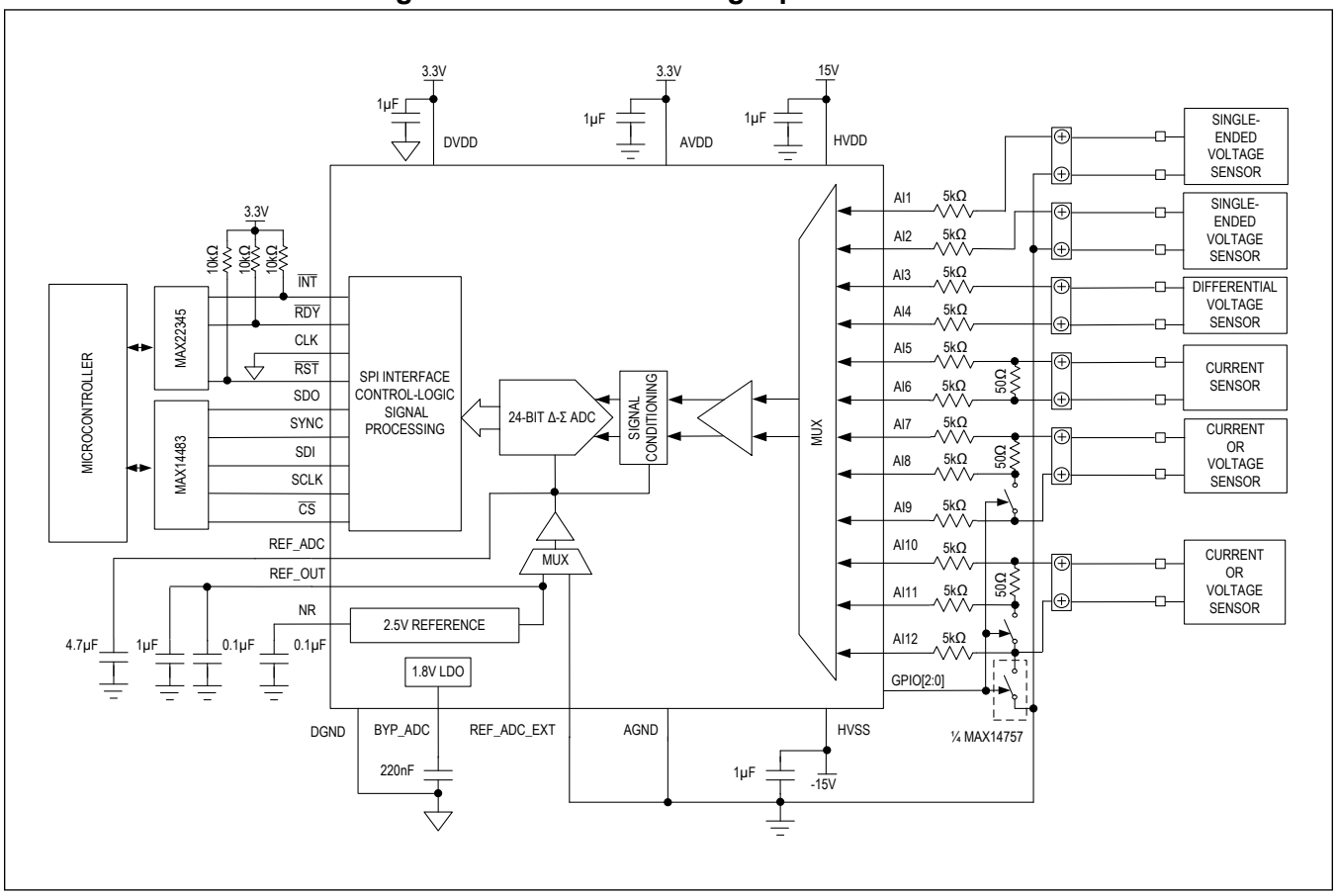
With external circuitry, the input ports are protected against ±2kV/42Ω surge pulses as per IEC61000-4-5. Place a minimum 4.7kΩ surge tolerant resistor in series with each analog input port.

The other MAX22005 pins are rated for a Human Body Model (HBM). If surge voltages can couple from the high voltage supplies (HVDD, HVSS) to the low-voltage supplies (DVDD or AVDD), place additional TVS suppressors on these power rails, or place TVS suppressors on the digital signal traces.

Each external sense resistor for current input mode (AICM) should be protected separately by an external TVS suppressor.

Typical Application Circuits

MAX22005 12-Channel Configurable Industrial Analog Input



Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	LEAD PITCH	ADC RESOLUTION
MAX22005ALM+	-40°C to +125°C	48-Pin LGA (7.5mm x 7.0mm)	0.5mm	24 bit
MAX22005ALM+T	-40°C to +125°C	48-Pin LGA (7.5mm x 7.0mm)	0.5mm	24 bit

+Denotes lead(Pb)-free/RoHS compliance.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Release for Market Intro	—