

MOSFET – Single N-Channel, POWERTRENCH®

100 V, 2.2 A, 243 mΩ

FDMA86108LZ

General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $r_{DS(on)}$ and gate charge provide excellent switching performance.

Features

- Max $r_{DS(on)}$ = 243 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 2.2\text{ A}$
- Max $r_{DS(on)}$ = 366 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 1.8\text{ A}$
- Low Profile – 0.8 mm Maximum in the New Package MicroFET™ 2 x 2 mm
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free and is RoHS Compliant

Application

- DC-DC Buck Converters

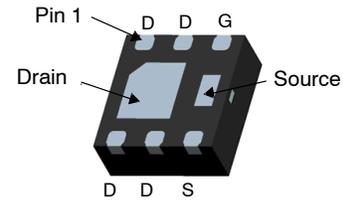
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	2.2	A
	– Pulsed (Note 3)	6	
P_D	Power dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	W
	Power dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	0.9	
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

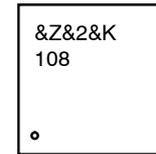
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	145	



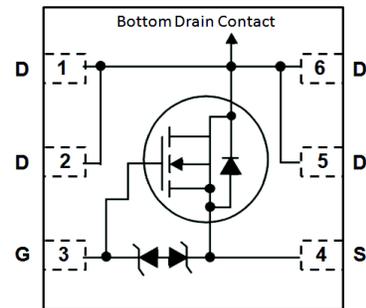
WDFN6 (MicroFET™ 2 x 2)
CASE 511CZ

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = Numeric Date Code
- &K = Lot Code
- 108 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMA86108LZ

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
108	FDMA86108LZ	WDFN6 (MicroFET 2x2) (Pb-Free)	3000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		74		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	2.2	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		-5		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 2.2 A		188	243	mΩ
		V _{GS} = 4.5 V, I _D = 1.8 A		275	366	
		V _{GS} = 10 V, I _D = 2.2 A, T _J = 125°C		345	446	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 2.2 A		3.7		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		116	163	pF
C _{oss}	Output Capacitance			23	35	
C _{rss}	Reverse Transfer Capacitance			1	5	
R _g	Gate Resistance		0.1	1.0	3.0	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn – On Delay Time	V _{DD} = 50 V, I _D = 2.2 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		4.2	10	ns
t _r	Rise Time			1.7	10	
t _{D(off)}	Turn – Off Delay Time			7.6	15	
t _f	Fall Time			1.7	10	
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0V to 10 V, V _{DD} = 50 V, i _D = 2.2 A		2.1	3.0	nC
		V _{GS} = 0V to 4.5 V, V _{DD} = 50 V, i _D = 2.2 A		1.1	1.6	
Q _{gs}	Gate to Source Charge	V _{DD} = 50 V, i _D = 2.2 A		0.5		
Q _{gd}	Gate to Drain “Miller” Charge			0.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

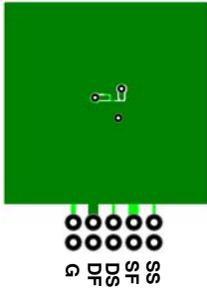
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.2 A (Note 2)		0.9	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 2.2 A, di/dt = 100 A/μs		32	51	ns
Q _{rr}	Reverse Recovery Charge			20	32	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDMA86108LZ

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



- a) 52°C/W when mounted on a 1 in² pad of 2 oz copper.



- b) 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Pulsed I_D measured at 250 μs, refer to Figure 11 SOA graph for more details.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

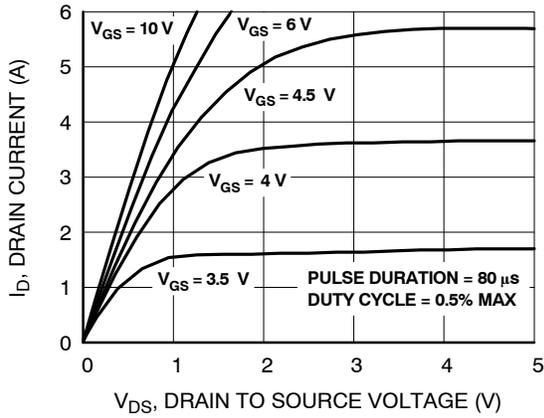


Figure 1. On-Region Characteristics

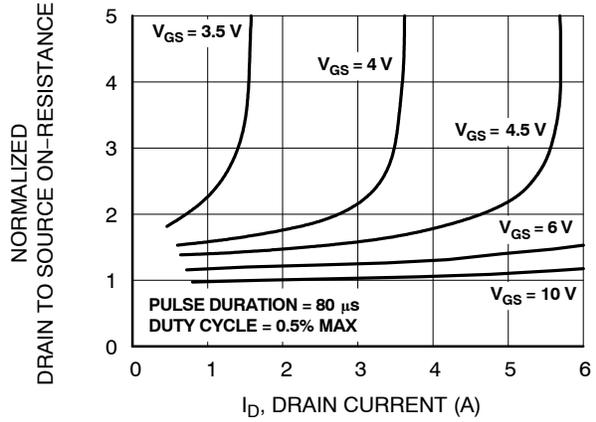


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

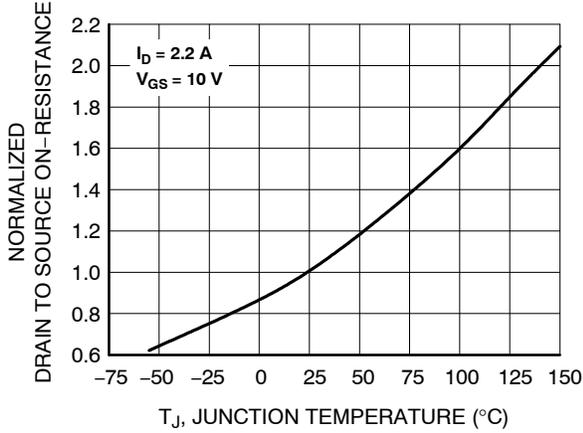


Figure 3. Normalized On-Resistance vs Junction Temperature

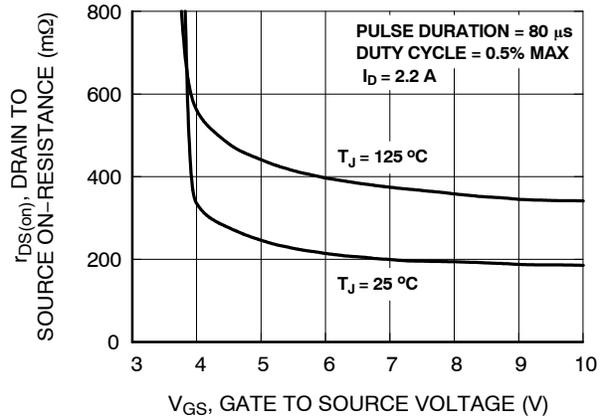


Figure 4. On-Resistance vs Gate to Source Voltage

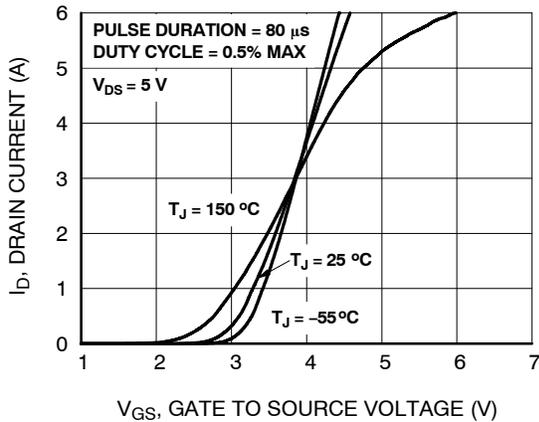


Figure 5. Transfer Characteristics

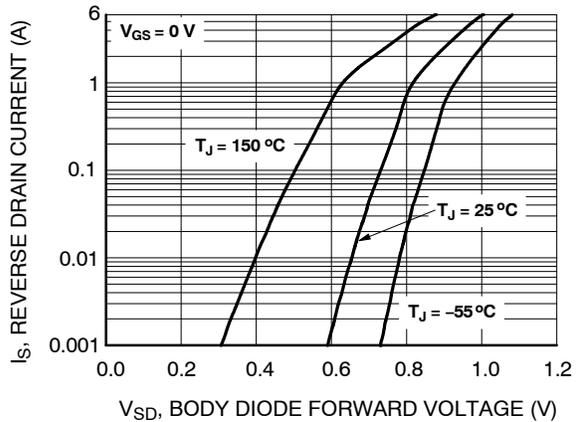


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

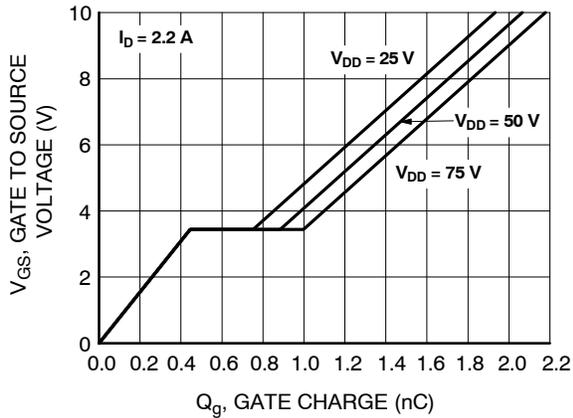


Figure 7. Gate Charge Characteristics

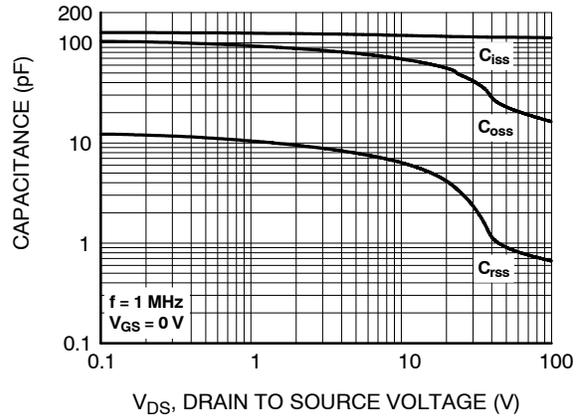


Figure 8. Capacitance vs Drain to Source Voltage

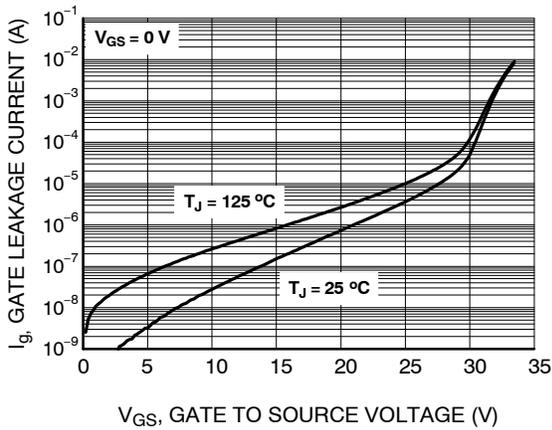


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

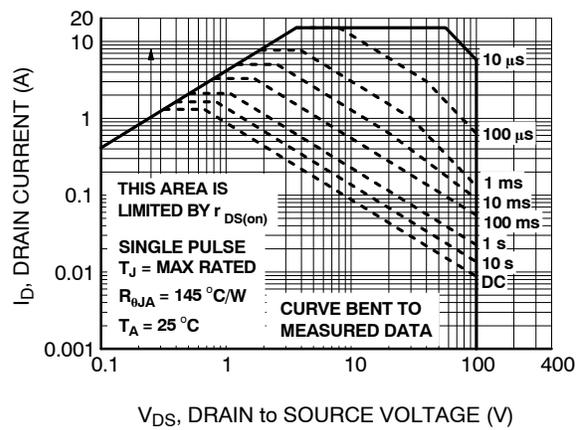


Figure 10. Forward Bias Safe Operating Area

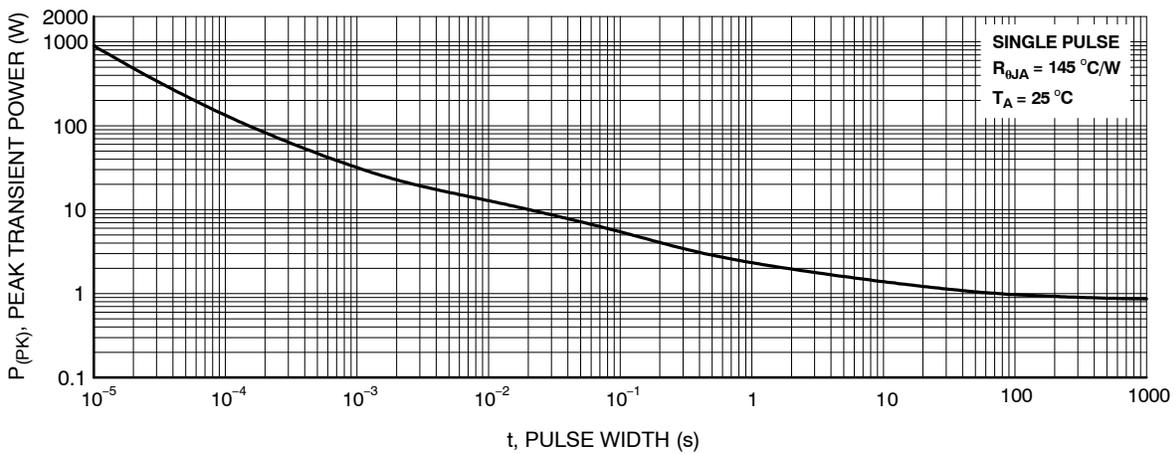


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

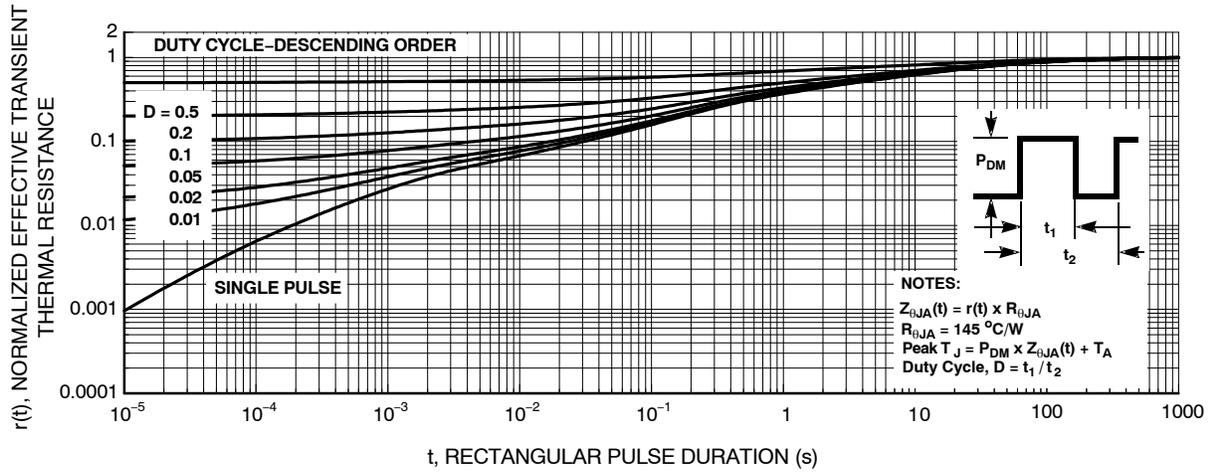


Figure 12. Junction to Ambient Transient Thermal Response Curve

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MECHANICAL CASE OUTLINE

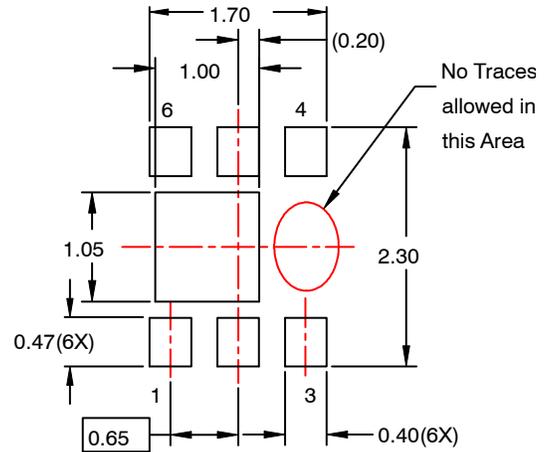
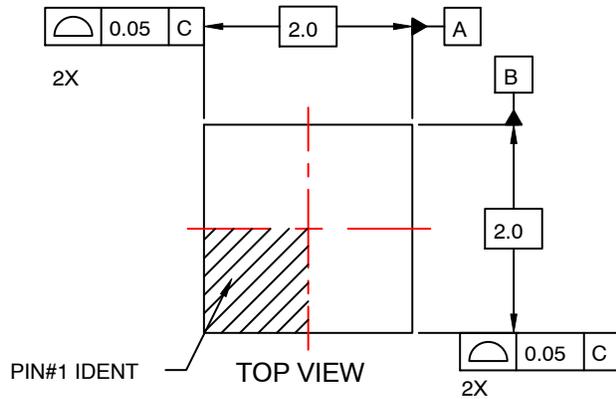
PACKAGE DIMENSIONS

ON Semiconductor®

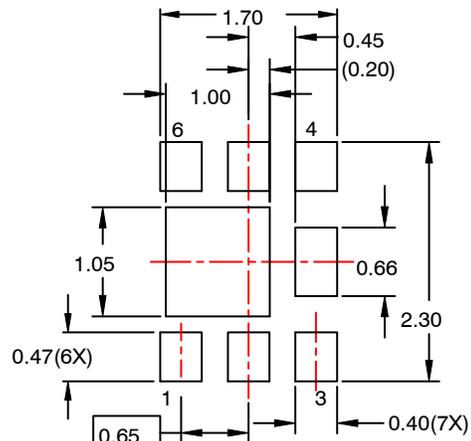
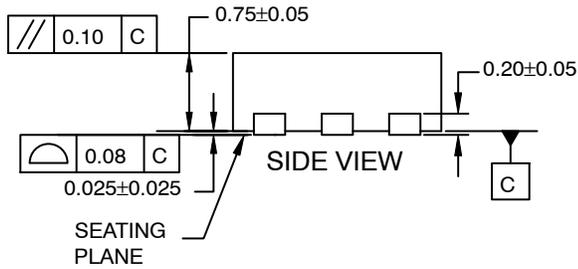


WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

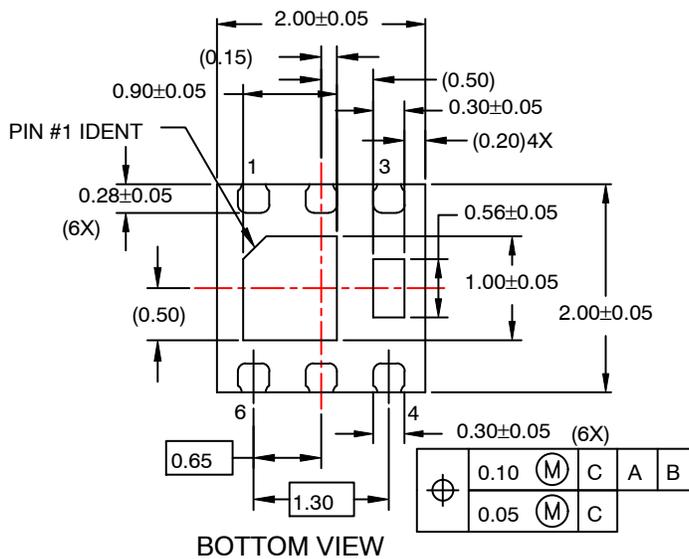
DATE 31 JUL 2016



RECOMMENDED
LAND PATTERN OPT 1



RECOMMENDED
LAND PATTERN OPT 2



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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